A Pulse-Tuned Charge Controlling Scheme for Uniform Main and Reference Bitline Voltage Generation on 1T1C FeRAM

Hee-Bok Kang, Hun-Woo Kye, Duck-Ju Kim, Geun-Il Lee, Je-Hoon Park, Jae-Kyung Wee
Seaung-Suk Lee, Suk-Kyoung Hong, Nam-Soo Kang and Jin-Yong Chung
Design Team, Memory R&D Center, Hyundai Electronics, Ichon, 467-701, Korea

Abstract

In order to improve cell array efficiency and reference voltage characteristics of 1T1C FeRAM, two key techniques are proposed in this paper. 1) Cell operation scheme with pulse-tuned signals on wordline and plateline for achieving uniform bitline levels in short time and 2) reference voltage generation scheme using dual pulse control for reference voltage to track variable bitline sensing voltage in wide range of operation voltage and temperature. 2Mb 1T1C FeRAM in unit block of 512 rows by 256 columns cell array with 0.35μm design rule are implemented.