Two schemes to reduce interconnect delay in bi-directional and uni-directional buses

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Abstract

As the device dimension is scaled down, interconnect RC delay becomes dominant performance limiter in high-performance VLSI's. Another issue is degradation of signal integrity, inducing delay fluctuation problems, due to a drastic increase of coupling capacitance. In this paper, a new buffer insertion scheme for bi-directional buses, namely dual-rail bus (DRB) scheme, and a high-speed buffer insertion scheme for uni-directional buses, namely staggered firing bus (SFB) scheme, are proposed and measured.