A 0.9-m A Standby Current DSP Core Using Improved ABC-MT-CMOS with Charge Pump Circuit

Hiromi Notani, Masayuki Koyama, Ryuji Mano,
Hiroshi Makino and Yoshio Matsuda

System LSI Development Center, Mitsubishi Electric Corporation
4-1 Mizuhara Itami Hyogo 664-8641 Japan
Phone:+81-727-84-7423, Fax:+81-727-84-7439, E-mail:shimada@lsi.melco.co.jp

Abstract

A 64-bit 80-MHz multimedia DSP core has been designed using 0.15-μm CMOS technology. An improved Auto-Backgate-Controlled MT-CMOS (ABC-MT-CMOS) circuit with a charge pump is adopted to suppress the standby leakage current. The dynamic active current of whole chip was simulated to optimize the size of the switch for the power supply control. The DSP core chip, which integrated 300-kgate Logic, 64-kbyte SRAM and charge pump circuit, has only 0.9-μA standby leakage current.