75 Word Abstract

Performance and Reliability of Ultra Thin CVD HfO_2 Gate Dielectrics with Dual Poly-Si Gate Electrodes

S. J. Lee, H. F. Luan, C. H. Lee, T. S. Jeon, W. P. Bai, Y. Senzaki*, D. Roberts*, and D. L. Kwong

Microelectronics Research Center, Department of Electrical and Computer Engineering, The University of Texas, Austin, TX 78712, (512)471-5749, Fax: (512)471-5625, sungjoo@mail.utexas.edu
*** Schumacher, Calsbad, CA 92009**

Abstract

MOSFETs with high quality ultra thin (EOT~10.3Å) HfO_2 gate stacks and self-aligned dual poly-Si gate are fabricated and characterized. Both n- and p-MOSFETs show good electron and hole mobility, respectively, and excellent sub-threshold swings. In addition, HfO_2 gate stack exhibits excellent thermal stability with poly-Si gate up to 1050°C/30s gate activation annealing and shows excellent TDDB reliability characteristics with negligible charge trapping and SILC under high-field stressing.