# A 0.15μm Logic based embedded DRAM technology featuring 0.425μm$^2$ Stacked Cell using MIM (Metal-Insulator-Metal) Capacitor

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We have developed embedded DRAM technology, in which 0.15μm logic transistor performance is fully compatible with that of pure logic process. The key technology is the newly developed MIM capacitor element having W/TiN/$Ta_2O_5$/TiN structure. This MIM capacitor element features that as low as 500℃ is sufficient for the formation process. Excellent leakage current characteristics of 8E-15A/μm$^2$@125℃ with $T_{eq}$(equivalent oxide thickness)=17Å has been obtained. This technology has been actually implemented into 4Mbit test chip with the cell size of 0.425μm$^2$. Over 50% yield without redundancy was obtained, confirming that there is no basic issue in process integration.