Effects of Gate-to-Body Tunneling Current on PD/SOI CMOS SRAM

In this paper, a detailed study on the effect of gate tunneling current on a high-performance 34 Kb L1 directory SRAM in a 1.5 V, 0.18um partially-depleted (PD)
SOI technology with Leff= 0.08 um and tox = 2.3 nm is presented.
This SRAM was originally designed in a 1.5 V, 0.18 um bulk CMOS technology and has achieved 2.0 GHz cycle time and 430 ps access time. It
utilizes pseudo-static circuits for robust timing and to facilitate migration to PD/SOI technology. The findings are - the presence of gat e-to-body tunneling current changes
the strength of individual cell transistor in the quiescent (standby) state,
thus affecting subsequent write/read operations. The degradation in the "Write" performance is more
significant than the degradation in the "Read" performance, and the effect is more
pronounced at lowered temperature. On the other hand, the
initial cycle "parasitic bipolar disturb" is reduced.