A 0.13-μm SOI CMOS Technology for Low-power and Digital Applications

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Abstract

Technologies that allow low-power digital and RF processing will enable future wireless, battery-operated electronic devices. We present a 0.13-μm, partially-depleted SOI CMOS technology with optimized power-saving and RF properties. Features include low-Vt FETs for minimum power dissipation and high performance at low voltage (25 ps inverter delay at 0.7 V Vdd), low-leakage high-Vt FETs, high NFET RF performance (141 GHz f_T and 98 GHz f_{max} at Vds = 1.2 V) and the following high-Q passives: inductors (simulated peak differential Q of 50 at L = 0.65 nH), MOS varactors, MIMCAPs and resistors.