A Fully Planalized 8M bit Ferroelectric RAM with ‘Chain’ Cell Structure

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A 8M-bit ferroelectric RAM (FeRAM) was successfully fabricated. For realizing low resistive (<10Ω/□) gate electrode after thermal process around the capacitor process, Co-salicide was suitable for our requirement. The 0.9um square Pt/SRO/PZT/SRO/Pt stacked structure promise high reliable operation. The low damage dual damascene process with Nb liner assisted aluminum reflow process was employed for avoiding degradation of ferroelectric capacitor during the matellization. To obtain high cell efficiency, ‘Chain’ cell structure was adopted.