A Binocular CMOS Range Image Sensor with Bit-Serial Block-Parallel Interface Using Cyclic Pipelined ADC's

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A binocular CMOS image sensor used with a pair of aligned-in-parallel optical systems for range imaging is implemented. Sixteen compact cyclic pipelined analog-to-digital converters are integrated per an image sensor. The dedicated processor starts 16 x 16 FFT when the first bit-serial block-parallel data is obtained. The image sensor produces a 16 x 16 range image from a pair of 256 x 256 images, together with the dedicated pipelined FFT processor, at the maximum pipeline performance.