A Leakage-Biased Domino circuit family is proposed that maintains high speed in active mode but which can be rapidly placed into a low-leakage inactive state by using leakage currents themselves to bias internal nodes. A 32-bit Han-Carlson domino adder circuit is used to compare LB-Domino with conventional single and dual Vt domino circuits. For equal delay and noise margin, the LB-Domino technique gives two decades reduction in steady-state leakage energy compared to a dual-Vt technique.