A Leakage-Tolerant Dynamic Register File Using Leakage Bypass with Stack Forcing (LBSF) and Source Follower NMOS (SFN) Techniques

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LBSF and SFN leakage-tolerant techniques improve robustness of leakage-sensitive and performance-critical wide dynamic circuits in the local and global bitlines of a 256X32b register file in a 100nm dual-V_T technology. The full LBSF design improves clock frequency by 50% or reduces energy by 37%, compared to the best dual-V_T (DVT) design. Performance advantages of LBSF and SFN become more significant as leakage increases.