

A 6bit 400Msps 70mW ADC Using Interpolated Parallel Scheme

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The design of a low power 6bit, 400Msps, 1.8V CMOS ADC is presented. This ADC is based on interpolated parallel architecture in which the transistor sizes are optimized to achieve the required linearity and simultaneously minimize the power consumption. When operated at 400Msps with 1.8/2.4V power supply the ADC dissipates 70mW. The ADC is fabricated in a 0.18 μ m CMOS process.