A 1.2 V 10-b 100-MSamples/s A/D Converter in 0.12 mm CMOS

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This paper describes the implementation of a 10-bit analog-to-digital converter (ADC). The converter utilizes techniques such as folding and distributed interpolation to reduce the required hardware. In addition resistive averaging is used to reduce the device sizes. Fabricated in a digital 0.12 µm CMOS process, the ADC occupies 0.32 mm^2 while dissipating 140 mW from a single 1.2 V supply. The experimental results show that the converter achieves 55dB SNR at sampling frequencies up to 100MHz.