A Floating-Gate Trimmed, 14-Bit, 250 Ms/s Digital-to-Analog Converter in Standard 0.25µm CMOS

John Hyde, Todd Humes, Chris Diorio, Mike Thomas, Miguel Figueroa

Impinj, Inc.
501 N. 34th Street, Suite 100, Seattle, WA 98103
Phone: +1 (206) 517–5300, Fax: +1 (206) 517–5262, Email: {john.hyde, todd.humes, diorio, mike.thomas, miguel}@impinj.com

We describe a floating-gate trimmed, 14-bit, 250Ms/s current-steered DAC fabricated in a 0.25µm CMOS logic process. We trim the static INL to ±0.3LSB using analog charge stored on floating-gate *p*FETs. The DAC occupies 0.44mm^2 of die area, consumes 53mW at 250MHz, allows on-chip electrical trimming, and achieves 72dB SFDR at 250Ms/s.