Programmable and Automatically-Adjustable Sense-Amplifier Activation Scheme and Multi-Reset Address-Driven Decoding Scheme for High-Speed Reusable SRAM Core

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We describe novel schemes developed to meet the demand for a reusable embedded SRAM core for application to a variety of SOC design. PAS optimizes Sense-amplifier activation timing by using the combination of a program and automatic control. MRAD minimizes timing-overhead by reducing the fluctuation of path-to-path delay. These schemes experimentally demonstrated a wide-operation range of 0.5 to 1.4 V and an access time of 600 ps.