Programmable Termination for CML I/O's in High Speed CMOS Transceivers

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This paper describes I/O circuits that can be used in high-speed transceivers to communicate with next generation and legacy devices. We describe the transmitter and receiver front-end circuits that are designed to operate with dual termination voltage supplies. The circuits are designed in a 0.18µm CMOS process having separate 1.8V and 3.3V transistors. A novel receiver characterization scheme, a new ESD protection circuit, and system level power up issues related to gate-oxide and electro-migration reliability is discussed.