Abstract

A 60nm gate length CMOS technology for high performance applications at the 0.13μm CMOS node is presented. The technology utilizes 193nm gate lithography, dual spacers with thin spacer before drain extension implant and L-shaped nitride spacer after drain extensions, and remote-plasma nitrided oxide with 1.75nm EOT. A 10-15% improvement in drive current is achieved with lower series resistance by reduction of dopant loss and higher dopant activation, resulting in n- and pMOS I_{drive} of 1000 μA/μm and 450 μA/μm at 1.2V at I_{off}= 50 nA/μm.