A New Double-Layered Structure for Mass-Production-Worthy CMOSFETs with Poly-SiGe Gate

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A new double-layered structure of poly-Si/SiGe gate has been proposed to improve the current performance of CMOSFETs and the reproducibility of devices. The double-layered poly-Si/SiGe stack has small-sized (columnar) grains in the lower poly-SiGe layer and large-sized grains in the upper poly-Si layer. The new structure can suppress Ge diffusion into the upper poly-Si layer during CMOS process, resulting in enhanced current performance and better sheet resistance distribution to meet gate height scaling requirements sub-0.1μm CMOSFETs. Mass productive 8M SRAM with both the smallest cell size and the enhanced operation speed by 20% was successfully fabricated using the proposed poly-SiGe gate structure.