Gate Postdoping to Decouple Implant/Anneal for Gate, Source/Drain, and Extension: Maximizing Polysilicon Gate Activation for 0.1 µm CMOS Technologies

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To maximize gate activation in sub-0.1 µm conventional CMOS devices, we introduce "Gate Postdoping" as the most efficient method to activate the poly gate by decoupling both implant and anneal for gate and source/drain. By successfully applying the method in 0.1 µm CMOS technologies for the first time, we achieved tremendous improvement in CMOS on-currents by 9 ~ 33% over a conventional process, reducing equivalent gate oxide thickness in inversion by up to ~2 Å.