75 Word Abstract

ELFIN (<u>EL</u>evated <u>Field IN</u>sulator) and SEP (<u>S/D Elevated by Poly-Si Plugging</u>) Process for Ultra-Thin SOI MOSFETs with High Performance and High Reliability

Jong-Wook Lee, Hisashi Takemura**, Yukisige Saitoh*, Risho Koh, Shigeharu Yamagami, Tohru Mogami, Mitsuyoshi Uto***, Nobuyuki Ikezawa***, and Nobuyuki Takasu****

Silicon Systems Research Labs., *R&D Technical Support Center, ***System LSI Operation Unit,

******ULSI Manufacturing Engineering Division., NEC Co.

1120, Shimokuzawa, Sagamihara, Kanagawa, 229-1198, Japan

**Present address: New Energy and Industrial Technology Development Organization (NEDO), Japan

ELFIN (<u>EL</u>evated <u>Field IN</u>sulator) process for device isolation and SEP (<u>S</u>/D <u>E</u>levated by <u>P</u>oly-Si Plugging) process for elevated S/D structure is developed for ultra-thin SOI MOSFETs with SOI film less than 20 nm. With ELFIN, reverse narrow channel effect of NMOSFET is improved by about 50 %, gate leakage current decreased by about 30 %, and hot-carrier immunity increased by about 20 %. With SEP, thick S/D region is obtained even with 20 nm SOI film so that S/D resistance is deceased to a third with excellent uniformity.