

Suppression of Leakage Current in SOI CMOS LSIs by Using Silicon-Sidewall Body-Contact (SSBC) Technology

Naoki Kotani, Satoru Ito, Takatoshi Yasui, Atsuo Wada, Toru Yamaoka and Takashi Hori

ULSI Process Technology Development Center, Matsushita Electric Industrial Co., Ltd.

19 Nishikujo-Kasugacho, Minami-Ku, Kyoto 601-8413, Japan

TEL: +81-75-662-8914, FAX: +81-75-662-6196, E-mail: nao@krl.mec.mei.co.jp

Abstract

This paper clarifies two SOI-specific leakage components, STI-induced punchthrough and gate-oxide leakage, found especially in large-scale integration, and proposes a new SOI technology: Silicon-Sidewall Body-Contact (SSBC). Without layout penalty and process complexity, SSBC realizes self-aligned body contact to the substrate, which suppresses gate-oxide leakage, and prevents the SOI body from being mechanically stressed, thus eliminating punchthrough leakage. SSBC is promising for scaled SOI CMOS LSIs.