

It was proven that the body-tied SOI technology with partial trench isolation (PTI) has high soft-error immunity. As compared with the bulk, a three-order reduction of the soft-error rate for a 0.18 μm SOI 4M-bit SRAM with the PTI was successfully realized. A design guideline to suppress soft errors is presented. Beyond 0.13 μm node, high soft-error immunity for the body-tied SOI device was projected as compared with the bulk as well as the body-floating SOI device.