

A 5-GHz CMOS Double-Quadrature Receiver for IEEE 802.11a Applications

Chung-Yu Wu and Chung-Yun Chou

Department of Electronics Engineering
National Chiao-Tung University, Hsin-Chu 300, Taiwan, R.O.C.

A 5-GHz CMOS double-quadrature front-end receiver for Wireless-LAN application is proposed. In the receiver, a one-stage RLC phase-shifter is used to generate quadrature RF signals and an active polyphase filter is designed to reject image signals. It has the advantages of low power dissipation, small chip area, and low sensitivity to parasitic components. Implemented in 0.18 μ m CMOS technology, the receiver chip can achieve 50.6dB image-rejection with the power dissipation of 22.4mW at 1.8-V voltage supply.