Low Jitter Butterworth Delay-Locked Loops

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Abstract

The low jitter Butterworth delay-locked loops (DLLs) are presented in this paper. The proposed Butterworth DLLs can suppress both the jitters generated by the input noise and the voltage-controlled delay line (VCDL) noise without stability considerations. Theoretically, the proposed Butterworth 2^{nd}-order DLL and 3^{rd}-order one could reduce the rms jitter due to the VCDL by a factor of $\sqrt{2}$ and 2, respectively. In addition, a technique called dynamic bandwidth-adjusting scheme (DBAS) is adopted to shorten the lock time without compromising the jitter performance. The conventional DLL and the proposed ones are simultaneously fabricated at the same die in a CMOS 0.35-um one-poly four-metal process. Compared with the conventional DLL, the measured rms jitters of the proposed DLLs can be improved by a factor of 1.40 and 1.95, respectively, with an input frequency of 125MHz. The maximum power consumption of the proposed DLLs is 32mW.