A Multiply-by-3 Coupled-Ring Oscillator for Low-Power Frequency Synthesis

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A frequency-synthesis technique which extracts the N^{th} harmonic from an N-stage oscillator is presented. The maximum achievable voltage swing from such an oscillator is estimated. To study this technique, a multiply-by-3 circuit with two 180^{o}-coupled, single-ended three-stage ring oscillators has been fabricated in 0.24 μm CMOS, designed to work in the 902-928 MHz ISM band (US and Canada). It provides two outputs: one at the normal operating frequency of the oscillator, and another at three times that frequency. The circuit can work at voltages as low as 1.3 V, while consuming 210 μA of current.