

This clock generation and distribution scheme enables Intel's first mobile-specific micro-architecture of Pentium® M (Banias) microprocessor. It employs four phase-locked loops, three of them cascaded, to generate the required clock frequencies, provide low skew and jitter and support the next-generation Intel SpeedStep® technology. The core clock distribution is implemented as two grids with an active continuous de-skewing mechanism. The debug capabilities of this clocking scheme provide easy observability and testing, enabling rapid time to market.