3-Dimensional Vertical Parallel Plate Capacitors in an SOI CMOS Technology for Integrated RF Circuits

Jonghae Kim[1], Jean-Olivier Plouchart[2], Noah Zamdmer[1], Melanie Sherony[1], Liang-Hung Lu[1], Yue Tan[1], Meeyoung Yoon[1], Keith A. Jenkins[2], Mahender Kumar[1], Asit Ray[1], Lawrence Wagner[1]

[1]IBM Semiconductor Research and Development Center, Hopewell Junction, NY 12533 USA
[2]IBM T.J. Watson Research Center, Yorktown Heights, NY 10598 USA
Phone:+1-845-892-9832, FAX:+1-845-892-6899, e-mail:jonghae@us.ibm.com

Abstract

This paper presents high-Q and high-density 3-dimensional VPP (vertical parallel plate) capacitors fabricated in a 0.12 μm SOI CMOS technology. An effective capacitance density of 1.76 fF/μm² is obtained. A quality-factor of 22 at 1 GHz is obtained for a 20 pF VPP capacitor. Also, a VPP capacitor model is proposed for the first time to design the VPP capacitor.