

0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization

Ramin Farjad-Rad, Hiok-Tiaq Ng, M.-J. Edward Lee, Ramesh Senthinathan, William J. Dally¹,
Anhtuyet Nguyen, Rohit Rathi, John Poulton, John Edmondson, James Tran, Hadi Yazdanmehr

Velio Communications Inc., Milpitas, CA 95035, USA.

Stanford University, Stanford, CA 94305, USA. ¹

Abstract: This paper presents a 622Mbps to 8Gbps transceiver in standard 0.13 μ m CMOS technology. Each receiver and transmitter macrocell has its dedicated clock multiplication unit (CMU) and clock/data recovery unit (CDR), providing simultaneous multi-rate operation for multiple lanes on a chip. The transmitter and receiver front-end use direct 4:1 multiplex and 1:4 demultiplexing, using multiple-phase quarter-rate clocks. An automatic phase offset cancellation scheme is used to eliminate the phase mismatch of the multiple clock phases. Each transceiver occupies an active area of less than 0.4mm² and consumes 150mW at maximum speed.

0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization

Ramin Farjad-Rad, Hiok-Tiaq Ng, M.-J. Edward Lee, Ramesh Senthinathan, William J. Dally¹,
Anh Tuyet Nguyen, Rohit Rathi, John Poulton, John Edmondson, James Tran, Hadi Yazdanmehr

Velio Communications Inc., Milpitas, CA 95035, USA.

Stanford University, Stanford, CA 94305, USA. ¹

Abstract: This paper presents a 622Mbps to 8Gbps transceiver in standard 0.13 μ m CMOS technology. Each receiver and transmitter macrocell has its dedicated clock multiplication unit (CMU) and clock/data recovery unit (CDR), providing simultaneous multi-rate operation for multiple lanes on a chip. The transmitter and receiver front-end use direct 4:1 multiplex and 1:4 demultiplexing, using multiple-phase quarter-rate clocks. An automatic phase offset cancellation scheme is used to eliminate the phase mismatch of the multiple clock phases. Each transceiver occupies an active area of less than 0.4mm² and consumes 150mW at maximum speed.

0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization

Ramin Farjad-Rad, Hiok-Tiaq Ng, M.-J. Edward Lee, Ramesh Senthinathan, William J. Dally¹,
Anhtuyet Nguyen, Rohit Rathi, John Poulton, John Edmondson, James Tran, Hadi Yazdanmehr

Velio Communications Inc., Milpitas, CA 95035, USA.

Stanford University, Stanford, CA 94305, USA. ¹

Abstract: This paper presents a 622Mbps to 8Gbps transceiver in standard 0.13 μ m CMOS technology. Each receiver and transmitter macrocell has its dedicated clock multiplication unit (CMU) and clock/data recovery unit (CDR), providing simultaneous multi-rate operation for multiple lanes on a chip. The transmitter and receiver front-end use direct 4:1 multiplex and 1:4 demultiplexing, using multiple-phase quarter-rate clocks. An automatic phase offset cancellation scheme is used to eliminate the phase mismatch of the multiple clock phases. Each transceiver occupies an active area of less than 0.4mm² and consumes 150mW at maximum speed.

0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization

Ramin Farjad-Rad, Hiok-Tiaq Ng, M.-J. Edward Lee, Ramesh Senthinathan, William J. Dally¹,
Anh Tuyet Nguyen, Rohit Rathi, John Poulton, John Edmondson, James Tran, Hadi Yazdanmehr

Velio Communications Inc., Milpitas, CA 95035, USA.

Stanford University, Stanford, CA 94305, USA. ¹

Abstract: This paper presents a 622Mbps to 8Gbps transceiver in standard 0.13 μ m CMOS technology. Each receiver and transmitter macrocell has its dedicated clock multiplication unit (CMU) and clock/data recovery unit (CDR), providing simultaneous multi-rate operation for multiple lanes on a chip. The transmitter and receiver front-end use direct 4:1 multiplex and 1:4 demultiplexing, using multiple-phase quarter-rate clocks. An automatic phase offset cancellation scheme is used to eliminate the phase mismatch of the multiple clock phases. Each transceiver occupies an active area of less than 0.4mm² and consumes 150mW at maximum speed.

0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization

Ramin Farjad-Rad, Hiok-Tiaq Ng, M.-J. Edward Lee, Ramesh Senthinathan, William J. Dally¹,
Anhtuyet Nguyen, Rohit Rathi, John Poulton, John Edmondson, James Tran, Hadi Yazdanmehr

Velio Communications Inc., Milpitas, CA 95035, USA.

Stanford University, Stanford, CA 94305, USA. ¹

Abstract: This paper presents a 622Mbps to 8Gbps transceiver in standard 0.13 μ m CMOS technology. Each receiver and transmitter macrocell has its dedicated clock multiplication unit (CMU) and clock/data recovery unit (CDR), providing simultaneous multi-rate operation for multiple lanes on a chip. The transmitter and receiver front-end use direct 4:1 multiplex and 1:4 demultiplexing, using multiple-phase quarter-rate clocks. An automatic phase offset cancellation scheme is used to eliminate the phase mismatch of the multiple clock phases. Each transceiver occupies an active area of less than 0.4mm² and consumes 150mW at maximum speed.

0.622-8.0Gbps 150mW Serial IO Macrocell with Fully Flexible Preemphasis and Equalization

Ramin Farjad-Rad, Hiok-Tiaq Ng, M.-J. Edward Lee, Ramesh Senthinathan, William J. Dally¹,
Anhtuyet Nguyen, Rohit Rathi, John Poulton, John Edmondson, James Tran, Hadi Yazdanmehr

Velio Communications Inc., Milpitas, CA 95035, USA.

Stanford University, Stanford, CA 94305, USA. ¹

Abstract: This paper presents a 622Mbps to 8Gbps transceiver in standard 0.13 μ m CMOS technology. Each receiver and transmitter macrocell has its dedicated clock multiplication unit (CMU) and clock/data recovery unit (CDR), providing simultaneous multi-rate operation for multiple lanes on a chip. The transmitter and receiver front-end use direct 4:1 multiplex and 1:4 demultiplexing, using multiple-phase quarter-rate clocks. An automatic phase offset cancellation scheme is used to eliminate the phase mismatch of the multiple clock phases. Each transceiver occupies an active area of less than 0.4mm² and consumes 150mW at maximum speed.