High Performance 25nm FDSOI Devices with Extremely Thin Silicon Channel

Z. Krivokapic, W. Maszara, F. Arasnia, E Paton, Y. Kim*, L. Washington*, E. Zhao, J. Chan, J. Zhang, A. Marathe, M-R. Lin

AMD, Technology Research Group,M/S 143, One AMD Place, Sunnyvale, CA 94088-3453, USA *Applied Materials, 3050 Bowers Av., Santa Clara, CA 95054, USA e-mail: Zoran.Krivokapic@amd.com

We achieve, for the first time, high performance FDSOI devices down to the 25nm with silicon channel thickness between 7 and 10nm. We use metal gate with undoped channel and raised source/drain with 12nm spacer. We report the highest PMOS drive current for a single-gate device ($I_{on}=789\mu A/\mu m$ and $I_{off}=27nA/\mu m$ for $V_{gs}-V_t=1.25V$). We report that thinner channels degrade mobility and excellent hot carrier and gate dielectric reliability.