Highly Stable 65nm Node (CMOS5) 0.56μm^2 SRAM Cell Design for Very Low Operation Voltage

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Abstract

This paper presents a very high density embedded SRAM technology for 65nm node (CMOS5). The SRAM cell size is 0.56μm^2, which is the smallest of all reported SRAM cells. This fabrication is fully compatible with CMOS logic technologies, using optimized optical proximity correction (OPC). This is achieved by double-patterning technique using high NA ArF lithography with complementary phase-shift and narrow well isolation. Furthermore, we investigated static noise margin and cell current for low power voltage.