Comparison of sub 1 nm TiN/HfO2 with Poly-Si/HfO_2 gate stacks using scaled chemical oxide interface

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Chemical oxide scaling by modulating ozone concentration is used to produce SiO_x interfaces with thickness as low as 0.3 nm for HfO_2 dielectrics deposition. Poly NMOS capacitors and conventional self-aligned transistors down to 65nm gate lengths with final EOT ranged from 1.2-1.8 nm were obtained. Sputtered TiN gate on the identical stacks yielded 0.82 nm EOT on NMOS devices using scaled chemical oxide interface with leakage current of 10^{-3} A/cm^{-2}.