CIRCUITS RUMP SESSION
Thursday, June 15
8:00 p.m. – 10:00 p.m.

Organizers: C.K. Ken Yang, UCLA
K. Kobayashi, Kyoto University

R1: Complete Integration of SoC Power Management - Reality or Mirage?
Organizers/Moderators: K. Gulati, BitWave Semi.
M. Hiraki, Renesas Technology

SoCs often employ a diverse set of circuits – RF, analog, digital, I/O, memory – each with a different set of demands on the supply voltage level, noise, loading and its adaptability to chip performance. Integrating supply converters improves form-factor, system yield, bill-of-materials and efficiency. Yet it is not clear how bulky inductors and large capacitors can be integrated cost effectively. How should these converters be modified to enable integration? How do battery voltage level and process technology influence the selection of converter architecture? Can switching regulators be used for powering sensitive RF and analog circuits? How will next generation energy sources influence power management? This panel will consider all of these issues and more in the context of SoCs for future portable devices.

Panelists:
S. Dosho, Matsushita
Y. Kanno, Hitachi
T. Karnik, Intel
K. Kunz, Texas Instruments
B. Miwa, Maxim Integrated
G. Rincón-Mora, Georgia Inst. of Tech

R2: What Will be the Next Embedded Memory Workhorse?
Honolulu II
Organizers: S. Natarajan, Emerging Memory Technologies, Inc.
K. Noda, N Score

Moderator: S. Natarajan, Emerging Memory Technologies, Inc.

6T-SRAM technology has been the dominant embedded memory of choice primarily due to its high performance, excellent CMOS compatibility, and manufacturing robustness. At 45nm and 32nm technology nodes, because of ever-increasing device variability and the need for transistor voltage down-scaling, the stability of 6T-SRAM cell becomes a significant issue that likely requires significant cell area penalty to overcome.

Alternative embedded memory technologies to 6T-SRAM have been the subject of research and development for many years. Few of these alternative technologies, however, have proven to be viable or have been able to match 6T-SRAM in high-performance applications. Thyristor-based memory (T-RAM) is emerging as an attractive embedded memory solution for 45nm and beyond, especially with the increasing adoption of process/device technologies such as SOI and FinFET in deep nano-scale CMOS.

T-RAM technology offers 6T-SRAM performance and functionality at more than twice the macro density, a simple process addition into a baseline SOI CMOS technology that involves extra implant steps only, and a straight-line layout that greatly simplifies lithography.

Panelists:
P. Rickert, TI
H. Pilo, IBM
T. Furuyama, Toshiba
S. Chung, TSMC
S. Rusu, Intel Corp.
F. Nemati, T-RAM Inc