TECHNOLOGY / CIRCUITS
JOINT RUMP SESSION
Wednesday, June 14
8:00 p.m. – 10:00 p.m.

Organizers: Shahin Sharifzadeh, Cypress Semi.
Renichi Yamada, Hitachi, Ltd.

RJ1 Power Management: What are the Device and Circuit Trade-offs. How Will it be Managed at 45nm and 32nm Nodes

Organizers:

Circuits	**Technology**
K. Nowka, IBM	H. Puchner, Cypress
Y. Oowaki, Toshiba	T. Ipposhi, Renesas

Moderator: T. Skotnicki, STMicroelectronics

Power management has historically focused on low standby and operating power for mobile devices to increase the battery time. In today's designs, it is increasingly important to optimize power for all electronic applications. Data centers can consume the power of small cities. Previous efforts for power reduction have been focusing on technology as well as design options to reduce standby power. However, it is not clear which of the options will be available in future designs and what other limitations will arise from these reduction techniques. The discussion panel is a compilation of design and process experts and will present views on power management for the 45-nm and 32-nm technology nodes. The panelists will present classical power reduction techniques such as gate leakage, sleeper transistors, cascading, fundamental improvements in leakage performance due to new device architectures. Various techniques will be debated on their merits for high-power vs low-power products or memory-intensive vs logic-dominated designs and technologies.

Panelists

Y. Urakawa, Toshiba
U. Ko, Texas Instruments
D. Frank, IBM
R. Kumar, Intel Corp
Y. Yamagata, NEC Electronics
D. Ditzel, Transmeta