SESSION 11 – TAPA II
Plenary Session II

Friday, June 16, 8:00 a.m.
Chairpersons: S. Kosonocky, IBM TJ Watson Research Center
K. Yano, Hitachi, Ltd.

11.1 – 8:00 a.m.
Through Silicon Via and 3-D Wafer/Chip Stacking Technology, Kenji Takahashi, Toshiba Corp.

11.2 – 8:45 a.m.
High Performance Processors in a Power Limited World, Sam Naffziger