SESSION 12 – TAPA I
Clock Generation and Distribution

Friday, June 16, 8:00 a.m.
Chairpersons: J. Farrell, AMD
M. Nagata, Kobe University

12.1 – 9:45 a.m.
17GHz Fine Grid Clock Distribution with Uniform-Amplitude Standing-Wave Oscillator, M. Sasaki, M. Shiozaki, A. Mori, A. Iwata, H. Ikeda*, Hiroshima University, Hiroshima, Japan, *Elpida Memory Inc., Kanagawa, Japan

This paper presents an inductive-loaded standing-wave clock oscillator. By coupling the oscillators into mesh structure, multi-ten GHz uniform-phase/amplitude global clocks can be distributed over a whole chip. In the mesh structure, finer grid can be employed than the conventional standing-wave technique, and it makes the depth of clock tree very shallow. We designed and fabricated a 17.2GHz oscillator in a 0.18um 6 metal CMOS technology. Low jitter less than 0.2% of the clock period has been achieved with 400um transmission line that was less than 1/10 of the conventional one. The power consumption was 13mW at 1.8V supply voltage.

12.2 – 10:10 a.m.
175 GMACS/mW Charge-Mode Adiabatic Mixed-Signal Array Processor, R. Karakiewicz, R. Genov, A. Abbas*, G. Cauwenberghs**, University of Toronto, Canada, *Johns Hopkins University, MD, **University of California, San Diego, CA

An adiabatic charge-recycling mixed-signal array with integrated resonant clock generator delivers 175 GMACS (multiply-and-accumulates per second) throughput for every mW of power, a ten-fold improvement over the dynamic power incurred when resonant line drivers are replaced with CMOS drivers. The 3-T CID/DRAM cell provides non-destructive 1b-1b multiply accumulation, and integrated quantizers yield 8-bit outputs with +/- 1 LSB worst-case mismatch. The 256x512 four-quadrant array is embedded in a processor for template-based face detection. Keywords: adiabatic, charge-recycling, matrix-vector multiplication, pattern recognition, mixed-signal and charge-mode.

12.3 – 10:35 a.m.
An On-chip Calibration Technique for Reducing Supply Voltage Sensitivity in Ring Oscillators, T. Wu, K. Mayaram, U.-K. Moon, Oregon State University, Corvallis, OR

A technique for reducing ring oscillator supply voltage sensitivity using on-chip calibration is described. A 1V 0.13um CMOS PLL demonstrates robust performance against VCO supply noise over operating frequencies of 500MHz-2GHz. The measured rms jitter of the proposed PLL with on-chip calibration is 4.4ps for an operating frequency of 1.4GHz in the presence of 10mV 1MHz VCO supply noise, while a conventional VCO measures 19.4ps rms jitter. The total power consumption of the PLL is 9.4mW, and the core die area of the PLL with calibration circuitry is 0.064mm^2.

12.4 – 11:00 a.m.
A 0.004mm^2 Portable Multiphase Clock Generator Tile for 1.2GHz RISC Microprocessor, I. Jung, G. Jung*, J. Song, M.-Y. Kim, J. Park*, S.B. Park*, C. Kim, Korea University, Seoul, Korea, *Samsung Electronics Corp., Yongin, Korea

A portable multiphase clock generator capable of adjusting its clock phase according to input clock frequencies has been developed. It consists of a full-digital CMOS circuit that leads to a simple, robust, and portable IP. One-cycle lock time enables clock-on-demand circuit structures. The implemented low power clock generator tile occupies only 0.004mm^2 and operates at variable input frequencies ranging from 625MHz to 1.2GHz.

12.5 – 11:25 a.m.
A Duty-Cycle Correction Circuit for High-Frequency Clocks, K. Agarwal, R. Montoye, IBM, Austin, TX

We present a circuit to control duty-cycle of high-frequency clocks with very fine resolution. The proposed duty-cycle detection and correction circuits are digital and do not require external references and matching devices. The circuits are designed to compensate for duty-cycle uncertainties in a floating point unit implemented using Limited Switch Dynamic Logic (LSDL) [1]. The results show that the circuit can correct the duty-cycle of an 8-GHz clock with +0.8% accuracy for an input range of 25% to 75%.