SESSION 13 – TAPA II
Non-Volatile Memory Architecture and Circuits

Friday, June 16, 9:45 a.m.
Chairpersons: H. Pon, Intel Corp.
T. Sekiguchi, Hitachi, Ltd.

13.1 – 9:45 a.m.
MRAM Cell Technology for Over 500MHz SoC, N. Sakimura, T. Sugibayashi, T. Honda, H. Honjo, S. Saito, T. Suzuki, N. Ishiwata, S. Tahara, NEC Corp., Kanagawa, Japan

We propose two new MRAM cell structures, 2T1MTJ and 5T2MTJ. Although they enable very high-speed operation, they require small-write-current magnetic tunnel junctions (MTJs). We found that write current could be reduced to 1mA by a novel MTJ into which a write line is inserted. The 5T2MTJ cell has two write current switches and a sense circuit. Simulation results show that access time of under 1ns is achieved when the magnetic resistance is 5k-ohm and its ratio (MR) is 150%.

13.2 – 10:10 a.m.
A Non-Volatile 2Mbit CBRAM Memory Core Featuring Advanced Read and Program Control, H. Hönigschmid, M. Angerbauer, S. Dietrich, M. Dimitrova, D. Gogl, C. Liaw, M. Markert, R. Symanczyk, L. Altimime, S. Bournat*, G. Müller, Infineon Technologies, Neubiberg, Germany, *Altis Semiconductor, Corbeil Essonnes, France

A 2Mbit CBRAM (Conductive Bridging Random Access Memory) core has been developed utilizing a 90nm, VDD = 1.5V process technology. The presented design uses an 8F2 (0.0648µm2) 1T1CBJ (1-Transistor/1-Conductive Bridging Junction) cell and introduces a fast feedback regulated CBJ read voltage and a novel program charge control using dummy cell bleeder devices. Random read/write cycle times <=50ns are demonstrated.

13.3 – 10:35 a.m.
The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories, H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi*, K. Tokami*, S. Kamohara*, O. Tsuchiya*, Hitachi Ltd., Tokyo, Japan, *Renesas Technology Corp., Tokyo, Japan

This paper describes for the first time the observation of the threshold voltage (Vth) fluctuation due to random telegraph signal (RTS) in flash memory. We acquired large-scale data of Vth fluctuation and confirm the existence of the tail bits generated by RTS. The amount of Vth broadening due to the tail bits becomes larger as the scaling advances, and reaches to more than 0.3 V in 45-nm node. Thus the RTS becomes prominent issue for the design of multilevel flash memory in 45-nm node and beyond.

13.4 – 11:00 a.m.
Design of 90nm 1Gb ORNAND™ Flash Memory with MirrorBit™ Technology, T.H. Kuo, N. Yang, N. Leong, E. Wang, F. Lai, A. Lee, H. Chen, S. Chandra, Y. Wu, T. Akaogi, A. Melik-Martirosian, A. Pourkeramati, J. Thomas, M. VanBuskirk, Spansion LLC, Sunnyvale, CA

Using the virtual ground array structure of 2 bits/cell MirrorBit technology, a 90nm, 1.8V ORNAND product combining the advantages of both NOR and NAND is presented. Full NAND functionality and performance compatibility is shown, while maintaining the NOR advantages. Keywords: NOR, NAND, Flash memory, MirrorBit, ORNAND.

13.5 – 11:25 a.m.
A Novel Program and Read Architecture for Contact-Less Virtual Ground NOR Flash Memory for High Density Application, N. Ito, Y. Yamauchi, N. Ueda, K. Yamamoto, Y. Sugita, T. Mineyama, A. Ishihama, K. Moritani, Sharp Corp., Nara, Japan

We have successfully developed multilevel contact-less Virtual ground array flash memory. Sequential program from the source side edge cell of each segment and 32cells unit program with data buffer enable to cancel the Vt interference between selected cell FG and neighboring cell FG. Sense amplifier assist equalize-sensing is implemented for high accuracy sensing operation. By these scheme, less than 85ns of access time for MLC read and 13.8us/word program time are obtained.