SESSION 14 – TAPA III
Serial Receivers

Friday, June 16, 9:45 a.m.
Chairpersons: K. Yang, University of California, Los Angeles
M. Mizuno, NEC Corp.

14.1 – 9:45 a.m.
A Fully Integrated 10Gbps Receiver with Adaptive Optical Dispersion Equalizer in 0.13µm CMOS, A. Momtaz, D. Chung, N. Kocaman, M. Caresosa, J. Cao, B. Zhang, I. Fujimori, Broadcom Corp., Irvine, CA

10Gbps receiver, containing adaptive equalizer, clock and data recovery, and demultiplexer, is implemented in 0.13µm CMOS. By compensating for optical dispersion, this chip recovers transmitted data after 200km of single-mode fiber at BER < 10-12. Use of analog equalizer with digital adaptation garners total power dissipation of 950mW.

14.2 – 10:10 a.m.
A Single Chip 2.5 Gbps CMOS Burst Mode Optical Receiver, W.-Z. Chen, R.-M. Gan*, National Chiao-Tung University, Hsin-Chu, Taiwan, *Industrial Technology Research Institute, Hsin-Chu, Taiwan

This paper describes the design of a 2.5 Gbps burst-mode optical receiver in a 0.18 µm CMOS process. Integrating both transimpedance amplifier and post limiting amplifier in a single chip, the input sensitivity of the optical receiver is about -18 dBm, and the response time is less than 50 ns. The overall transimpedance gain is 98 dBΩ, and the -3 dB bandwidth is about 1.85 GHz. Operating under a single 1.8 V supply, this chip dissipates only 122 mW.

14.3 – 10:35 a.m.
A 35-Gb/s Limiting Amplifier in 0.13um CMOS Technology, C. Lee, S.-I. Liu, National Taiwan University, Taipei, Taiwan

A 35Gb/s limiting amplifier using cascaded- distributed amplifiers with active feedback and on-chip transformers achieves a differential gain SDD21 of 38 dB and a bandwidth of 26.2GHz. It has been fabricated in 0.13um CMOS technology. It exhibits a single-ended output swing of 300mVPP while consuming 125mW from a 1.5V supply.

14.4 – 11:00 a.m.
A 100-Gb/s 1:2 Demultiplexer, Y. Suzuki, M. Mamada, Z. Yamazaki, NEC Corp., Kanagawa, Japan

A 100-Gbit/s 1:2 demultiplexer (DEMUX) has been developed using InP HBT technology. The IC features broadband impedance matching with double terminations and transmission lines with a low phase constant in the data and clock distributions to obtain high signal quality and a large timing margin. Excellent eye diagrams with 550-mVp-p output voltage swings and 600-fs rms jitter were obtained. To the best of our knowledge, this is the highest data rate operation yet reported. Moreover, error-free operation for 231-1 at 100-Gb/s has been achieved.

14.5 – 11:25 a.m.
WITHDRAWN