SESSION 15 – TAPA I
SRAM Architecture and Techniques

Friday, June 16, 1:30 p.m.
Chairpersons: S. Butler, AMD
C. Kim, Samsung Electronics Co., Ltd.

15.1 – 1:30 p.m.
The 65nm 16MB On-die L3 Cache for a Dual Core Multi-Threaded Xeon® Processor, J. Chang, M. Huang, J. Shoemaker, J. Benoit, S.-L. Chen, W. Chen, S. Chiu, R. Ganesan, G. Leong, V. Lukka, S. Rusu, D. Srivastava, Intel Corp., Santa Clara, CA

The 16-way set associative, single-ported 16MB cache for the dual-core Xeon® Processor uses a 0.624um^2 cell in a 65nm 8-metal technology. Only 0.8% of the cache is powered up for an access. Sleep transistors are used in the SRAM array and peripherals. Dynamic Pellston with a history buffer protects the cache from latent defects and infant mortality failures.

15.2 – 1:55 p.m.
A SRAM Core Architecture with Adaptive Cell Bias Scheme, H.-S. Yu, N.-S. Kim, Y.-J. Son, Y.-G. Kim, H.-C. Kim, U.-R. Cho, H.-G. Byun, Samsung Electronics, Kyeonggi-Do, Korea

This paper describes an adaptive cell bias scheme that is proposed to achieve high performance and stability for a low power, high speed, and high density SRAM core with less process variation. The proposed scheme is featured with constrained-successive cell bias optimization method that determines the optimal cell bias condition sequentially to meet both the speed and stability target of a given SRAM core. The architecture with adaptive cell bias scheme is applied to a 144Mb double stacked S3 SRAM and leads to 49% reduction in SRAM core performance parameter variations with 8% area overhead. The power reduction is 21%.

15.3 – 2:20 p.m.
A 65 nm Ultra-High-Density Dual-port SRAM with 0.71um^2 8T-cell for SoC, K. Nii, Y. Masuda*, M. Yabuuchi*, Y. Tsukamoto, S. Ohbayashi, S. Imaoka*, M. Igarashi, K. Tomita, N. Tsuboi, H. Makino, K. Ishibashi, H. Shinohara, Renesas Technology Corp., Hyogo, Japan, *Renesas Design Corp., Hyogo, Japan

We propose a new access scheme of synchronous dual-port (DP) SRAM that minimizes area of 8T-DP cell and keeps cell stability. A priority row decoder circuit and shifted bit-line access scheme eliminates access conflict problem. Using 65nm CMOS technology (hp90), we fabricated 32KB DP-SRAM macros with the proposed scheme. We obtain 0.71um^2 8T-DP-cell, which cell size is 1.44x larger than 6T-single-port (SP)-cell.

15.4 – 2:45 p.m.
Self-Repairing SRAM for Reducing Parametric Failures in Nanoscaled Memory, S. Mukhopadhyay, K. Kim, H. Mahmoodi*, A. Datta, D. Park, K. Roy, Purdue University, West Lafayette, IN, *San Francisco State University, San Francisco, CA

We present a self-repairing SRAM to reduce parametric failures using an on-chip leakage sensor and application of proper body bias. Simulations in a predictive 70nm technology show 5-40% (depending on inter-die Vt variation) improvement in SRAM yield. A test-chip is fabricated and measured in 0.13µm CMOS to demonstrate operation of the self-repair system.