SESSION 18 – TAPA I
Digital Processing

Friday, June 16, 3:25 p.m.
Chairpersons: K. Nowka, IBM
M. Ikeda, University Tokyo

18.1 – 3:25 p.m.
A 0.79mm^2 29mW Real-Time Face Detection Core, Y. Hori, M. Kusaka, T. Kuroda, Keio University, Yokohama, Japan

A 0.79mm^2 29mW real-time face detection core is fabricated in a 0.13µm CMOS technology. It consists of 75kgate logic, 58kbit SRAM, and the ARM AMBA bus interface. Comprehensive optimization in both algorithm and hardware design improves performance and reduces area and power dissipation significantly. The core can detect 8 faces per frame at 30fps. Face detection accuracy is 92%.

18.2 – 3:50 p.m.
1.047GHz, 1.2V, 90nm CMOS, 2-Way VLIW DSP Core Using Saturation Anticipator Circuit, H. Suzuki, H. Takata, H. Shinohara, E. Teraoka, M. Matsuo, T. Yoshida, H. Sato, N. Honda, N. Masui, T. Shimizu, Renesas Technology Corp., Itami, Japan

1.047GHz synthesizable 2-way VLIW General Purpose DSP core has been developed by 1.2V 90nm CMOS technology. The key technology is to detect saturation from adder's inputs in an ALU and parallelize the saturation check with the adder operation. The proposed saturation anticipator circuit and the logic structure optimization improve DSP's clock frequency by 20.8%. The test chip also runs 0.10uW/MHz at 0.8V low power operation mode.

18.3 – 4:15 p.m.
A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency, B. Zhai, L. Nazhandali, J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, D. Blaauw, T. Austin, University of Michigan, Ann Arbor, MI

A 2.6pJ/Inst subthreshold sensor processor designed for energy efficiency has been fabricated. A two-stage micro-architecture was implemented to mitigate the impact of process variation in subthreshold operation. Careful library cell selection and robust SRAM design enabled fully functional operation from 1.2V to 200mV. We analyze the variation in frequency and optimal voltage and evaluate the need for adaptive control. The processor reaches maximum energy efficiency at 360mV, consuming 2.6pJ/Inst at 833kHz. The minimum energy consumption of the core marks a 10X improvement over previous sensor processors at the same MIPS.

18.4 – 4:40 p.m.
A Watchdog Sensor for Assuring the Quality of Various Perishables with Subthreshold CMOS Circuits, K. Ueno, T. Hirose, T. Asai, Y. Amemiya, Hokkaido University, Hokkaido, Japan

We developed a CMOS integrated-circuit sensor that emulates the change in quality of various perishables. This sensor is attached to perishable goods such as farm and marine products and is carried from producers to consumers along with the goods. During their distribution process, the sensor experiences the surrounding temperature and emulates the deterioration of the goods caused by the surrounding temperatures. By reading the output of the sensor, consumers can determine whether the goods are fresh or not. This sensor consists of subthreshold CMOS circuits with a low-power consumption of 5 uW or less.

18.5 – 5:05 p.m.
A 70GOPS, 34mW Multi-Carrier MIMO Chip in 3.5mm^2, D. Markovic, R.W. Brodersen, B. Nikolic, Univ. of California, Berkeley, CA

An ASIC realization of the MIMO baseband processing for a multi-antenna WLAN is described. The chip implements a 4x4 adaptive singular value decomposition (SVD) algorithm with combined power and area minimization achieving a power efficiency of 2.1GOPS/mW in just 3.5mm2 in a 90nm CMOS. The computational throughput of 70GOPS is implemented with 0.5M gates at a 100MHz clock and 385mV supply, dissipating 34mW of power. With optimal channel conditions the algorithm implemented can deliver up to 250Mbps over 16MHz band.