SESSION 19 – TAPA II
Oversampled ADCs

Friday, June 16, 3:25 p.m.
Chairpersons: K. Nakamura, Analog Devices
S. Sugawa, Tohoku University

19.1 – 3:25 p.m.
A 0.9V 92dB Double-Sampled Switched-RC ΔΣ Audio ADC, M.G. Kim, G.-C. Ahn, P.K. Hanumolu, S.-H. Lee*, S.-H. Kim*, S.-B. You*, J.-W. Kim*, G.C. Temes, U.-K. Moon, Oregon State University, Corvallis, OR, *Samsung Electronics, Yongin, Korea

A 0.9V third-order 1.5bit Δ-Σ ADC with simple dynamic element matching is presented. A fully-differential low-voltage double-sampling structure avoids use of clock boosting or bootstrapping. It operates from 0.65V to 1.5V supply with minimal performance degradation. The prototype IC implemented in a 0.13um CMOS process achieves 92dB DR, 91dB SNR and 89dB SNDR, while consuming 1.5mW from a 0.9V supply.

19.2 – 3:50 p.m.
A 1.2V, 10.8mW, 500kHz Sigma-Delta Modulator with 84dB SNDR and 96dB SFDR, C.W. Tsang, Y. Chiu*, B. Nikolic, Univ. of California, Berkeley, CA, *University of Illinois, Urbana-Champaign, IL

A 1.2V switched-capacitor Σ-Δ modulator achieves 96dB peak SFDR and 84dB peak SNDR at 1MS/s in a 0.13um 6M1P general-purpose CMOS process. The high linearity is achieved by using high-gain op-amps and bootstrapped sampling switches. The power dissipation is 10.8mW at 64MHz clock frequency, excluding the voltage references.

19.3 – 4:15 p.m.
A 14-bit 5MS/s Continuous-Time Delta-Sigma A/D Modulator, Z. Li, T.S. Fiez, Oregon State University, Corvallis, OR

A continuous-time Δ-Σ A/D modulator providing 85dB DR with 5MS/s output rate in a 2.5V 0.25μm CMOS process is presented. The modulator has a single-stage, dual-loop architecture allowing nearly one clock period excess loop delay. A multi-bit quantizer is used to increase resolution and non-return-to-zero DACs are adopted to reduce clock jitter sensitivity. Capacitor tuning is utilized to overcome process variation. Calibration is implemented to suppress DAC mismatch. Clocked at 60MHz, the chip consumes 50 mW.

19.4 – 4:40 p.m.
An 11-bit 330MHz 8X OSR Σ-Δ Modulator for Next-Generation WLAN, J. Paramesh[1,2], R. Bishop[2], K. Soumyanath[2], D. Allstot[1], [1]University of Washington, Seattle, WA, [2]Intel Corp., Hillsboro, OR

A 2-2 cascaded Σ-Δ modulator with 4-bit internal quantizers digitizes WLAN signals with 40MSPS conversion rate. Implemented in 90nm CMOS using nominal-Vt devices and metal comb capacitors, it occupies 1.3mm^2 core area, achieves 67dB, 63dB peak SNDR and 67dB peak SFDR at 330MHz, and dissipates 78mW from a 1.4V supply.

19.5 – 5:05 p.m.
A 4GHz 4th-order Passive LC Bandpass Delta-Sigma Modulator with IF at 1.4GHz, L. Luh, J.F. Jensen, C.-M. Lin, C.-T. Tsen, D. Le, A.E. Cosand, S. Thomas, C. Fields, HRL Laboratories LLC, Malibu, CA

A 4th-order bandpass Δ-Σ modulator utilizes a passive LC continuous-time architecture to achieve high IF frequency. A novel 3-bit noise-shaped quantizer is used to improve wideband performance with minimal distortion and loop delay. Eight 2nd-order LC modulators are used for noise shaping with minimal transistor count and power consumption. Implemented with 5195 InP HBT transistors, this modulator achieved 76dB SNR in 1 MHz bandwidth at 1.4GHz with a 4GHz sample rate.