SESSION 22 – TAPA II
Equalization Techniques

Saturday, June 17, 8:30 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
T. Sekiguchi, Hitachi, Ltd.

22.1 – 8:30 a.m.
A 5-mW 6-Gb/s Quarter-Rate Sampling Receiver with a 2-Tap DFE Using Soft Decisions, K.-L.J. Wong, A. Rylyakov*, C.-K.K. Yang, University of California, Los Angeles, CA, *IBM T J. Watson Research Center, Yorktown Heights, NY

A low-power quarter-rate sampling 2-tap DFE is realized for short I/O links. An analog sampling and soft-decision technique is used instead of look-ahead architectures to relax the critical path, and thus saving the power from the redundant paths. No errors are observed with 2^{31-1} PRBS at 6Gb/s, with 80-mV differential launch amplitude through a channel with 6.2-dB attenuation at 3GHz. The receiver draws 4.8mA from a 1.0-V supply.

22.2 – 8:55 a.m.
A Low-Power Receiver with Switched-Capacitor Summation DFE, A. Emami-Neyestanak, A. Varzaghani*, J. Bulzacchelli, A. Rylyakov, C.-K.K. Yang*, D. Friedman, IBM T.J. Watson Research Center, Yorktown Heights, NY, *University of California, Los Angeles, CA

A low power receiver with a one tap DFE was fabricated in 90nm CMOS technology. The speculative equalization is performed using switched-capacitor-based addition at the front-end sample-hold circuit. In order to further reduce the power consumption, an analog multiplexer is used in the speculation technique implementation. A quarter–rate-clocking scheme facilitates the use of low-power front-end circuitry and CMOS clock buffers. At 10Gb/s data rate, the receiver consumes less than 6.0mW from a 1.0V supply.

22.3 – 9:20 a.m.
A 10-Gb/s CMOS Merged Adaptive Equalizer/CDR Circuit for Serial-Link Receivers, S. Gondi, B. Razavi, University of California, Los Angeles, CA

A merged equalizer/CDR circuit employs a parallel-path equalizer and triple-loop adaptation to achieve a binary data rate of 10 Gb/s. Realized in 0.13-um CMOS technology, the circuit adapts to FR4 trace lengths up to 24 inches with BER<10^{-13} while consuming 133 mW from a 1.6-V supply.

22.4 – 9:45 a.m.
A 200Mb/s-2Gb/s Oversampling RX with Digitally Self-Adapting Equalizer in 0.18µm CMOS Technology, G.W. den Besten, F. Gerfers*, J. Conder*, A.J. Köllmann*, P. Petkov*, Philips Research, Eindhoven, The Netherlands, *Philips Semiconductor, Eindhoven, The Netherlands

This paper presents a 6x OSR receiver for serial data streams of 200Mb/s to 2Gb/s. An adaptive equalizer which is auto-calibrating on sample data statistics makes this receiver suitable for channels with large unknown losses. This robust and highly digitized receiver is demonstrated in 0.18um CMOS and can equalize variable cable losses up to 22dB. The self-adaptive equalizer part occupies only 0.08mm^2 and consumes 9-16mW.

22.5 – 10:10 a.m.
A Tunable Passive Filter for Low-Power High-speed Equalizers, R. Sun, J. Park, F. O'Mahony*, C. P. Yue, Carnegie Mellon University, Pittsburgh, PA, *Intel Corp., Hillsboro, OR

This paper presents the design and implementation of an integrated tunable passive filter for low-power continuous-time adaptive equalization. Based on a broadband matched high-pass filter topology, a PMOS biased in linear region is used to adjust the low-frequency attenuation for equalizing channel losses. A 0.13-um prototype demonstrates gain compensation up to 17 dB at 5 GHz without any power consumption.