Saturday, June 17, 10:50 a.m.
Chairpersons: K. Roy, Purdue University
                K. Kobayashi, Kyoto University

24.1 – 10:50 a.m.
Supply Voltage Adjustment Technique for Low Power Consumption and its Application to SOCs with Multiple Threshold Voltage CMOS, H. Okano, T. Shiota, Y. Kawabe, W. Shibamoto, T. Hashimoto, A. Inoue, Fujitsu Laboratories Ltd., Kawasaki, Japan

An energy-saving system for SOCs using multiple threshold voltage CMOS was developed. It equips process sensors and process-voltage conversion table generated from static timing analysis results, and adjusts the supply voltage according to die-to-die process variation. We applied this system to an embedded dual-core microprocessor using 90nm triple threshold voltage CMOS technology. When the microprocessor executes video stream decoding program, 17% power reduction was measured with dies of typical process condition.

24.2 – 11:15 a.m.
The Circuits and Robust Design Methodology of the Massively Parallel Processor Based on the Matrix Architecture, H. Noda, T. Tanizaki, T. Gyohten, K. Dosaka, M. Nakajima, K. Mizumoto, K. Yoshida, T. Iwao, T. Nishijima, Y. Okuno, K. Arimoto, Renesas Technology Corp., Hyogo, Japan

A novel circuits and design methodology of the massively parallel processor based on the matrix architecture is introduced. Unique circuit design of the parallel fine-grained processing elements enhances the performance of MAC (Multiply-Accumulate) operation up to 30.0GOPS/W. Hierarchical memory architecture with super wide internal bus and distributed power management contribute to the enhancement of the processing efficiency and the robustness of the macro. The proposed circuit design methodology proposed in this paper is especially effective for realizing high-performance, robust processing macro employed in SoCs.

24.3 – 11:40 a.m.
A Power-Managed Protocol Processor for Wireless Sensor Networks, M. Sheets, F. Burghardt, T. Karalar, J. Ammer, Y.H. Chee, J. Rabaey, University of California, Berkeley, CA

Wireless sensor network applications, such as environmental control in smart building and ecological monitoring, require low-power nodes that operate their entire lifetime without changing batteries. This paper describes the power management architecture for a digital protocol processor for a sensor network node. Eight subsystems implement the baseband through application protocol layers and are controlled by a centralized power manager. The prototype chip, implemented in 130nm CMOS, operates at 1.0V with an average power consumption of 150µW during normal operation.

24.4 – 12:05 p.m.
A Leakage Management System Based on Clock Gating Infrastructure for a 65-nm Digital Base-Band Modem Chip, F. Jumel, P. Royannez, H. Mair, D. Scott, A.E. Rachidi, R. Lagerquist, M. Chau, S. Gururajarao, S. Thiruvengadam, M. Clinton, V. Menezes, R. Hollingsworth, J. Vaccani, F. Piacebello, N. Culp, J. Rosal, M. Ball, F. Ben-Amar, L. Bouetel, O. Domerego, J.L. Lachese, C. Fournet-Fayard, J. Ciroux, C. Raibaut, U. Ko, Texas Instruments Inc., Villeneuve Loubet, France

In this paper we present a leakage management system which takes advantage of the existing clock gating infrastructure. This methodology avoids both RTL and software changes, at the block and chip level. We illustrate this approach with a 65-nm digital base band modem while achieving standby leakage in the 100-uA range and overall 1200X leakage reduction including process, circuit and system optimization.

24.5 – 12:30 p.m.
Distributed Active Decoupling Capacitors for On-Chip Supply Noise Cancellation in Digital VLSI Circuits, J. Gu, R. Harjani, C. Kim, University of Minnesota, Minneapolis, MN

A distributed active decoupling capacitor (decap) circuit is proposed to suppress the on-chip power supply noise in digital VLSI circuits. Effectiveness on suppressing local supply noise is verified from a 0.18µm test chip using multiple on-chip supply noise generators and supply noise sensors. Measurements show 4-11X boost in decap value over conventional passive decaps for frequencies up to 1GHz. Decap area reduction of 40% is achieved.