SESSION 3 – TAPA III
Image Sensors

Thursday, June 15, 10:00 a.m.
Chairpersons: T. Blalock, University of Virginia
S. Sugawa, Tohoku University

3.1 – 10:00 a.m.
WITHDRAWN -

3.2 – 10:25 a.m.
A 76 x 77mm^2, 16.85 Million Pixel CMOS APS Image Sensor, S.U. Ay, E.R. Fossum*, Micron Technology Inc., Pasadena, CA, *University of Southern California, Los Angeles, CA

A 16.85 million pixel (4,096 x 4,114), single die (76mmx77mm) CMOS active pixel sensor (APS) image sensor with 1.35Me- pixel well-depth was designed, fabricated, and tested in a 0.5µm CMOS process with a stitching option. A hybrid photodiode-photogate (HPDPG) APS pixel technology was developed. Pixel pitch was 18µm. The developed image sensor was the world's largest single-die CMOS image sensor fabricated on a 6-inch silicon wafer.

3.3 – 10:50 a.m.
A 3500fps High-Speed CMOS Image Sensor with 12b Column-Parallel Cyclic A/D Converters, M. Furuta, T. Inoue*, Y. Nishikawa, S. Kawahito, Shizuoka Univ., Hamammatsu, Japan, *Photron Ltd., Tokyo, Japan

This paper presents a high-speed CMOS image sensor with a global electronic shutter and 12bit column parallel cyclic A/D converters. The fabricated chip in 0.25um CMOS imager technology achieves the full frame rate in excess of 3500 frames per second. The in-pixel charge amplifier achieves the optical sensitivity of 19.9V/lx-s with on-chip microlens.

3.4 – 11:15 a.m.
A 0.88nW/pixel, 99.6 dB Linear-Dynamic-Range Fully-Digital Image Sensor Employing a Pixel-Level Sigma-Delta ADC, Z. Ignjatovic, M.F. Bocko, University of Rochester, Rochester, NY

We describe a CMOS image sensor employing pixel-level sigma-delta analog to digital conversion. The design has high fill factor (31%), zero DC offset fixed pattern noise and reduced reset and transistor readout noise in comparison to other analog and digital imager readout techniques. The sigma-delta pixel design also has low power consumption: 0.88 nW/pixel at 30 fps, high dynamic range of 16 bits, intrinsic linearity, and relative insensitivity to process variations.

3.5 – 11:40 a.m.
A High Dynamic Range CMOS Image Sensor with In-Pixel Floating-Node Analog Memory for Pixel Level Integration Time Control, S.-W. Han, S.-J. Kim, J.-H. Choi*, C.-K. Kim, E. Yoon*, KAIST, Daejeon, Korea, *University of Minnesota, Minneapolis, MN

In this paper we report a high dynamic range CMOS image sensor (CIS) with in-pixel floating-node analog memory for pixel level integration time control. Each pixel has different integration time based upon the amount of its previous frame illumination. There is no significant additional hardware because we use a floating-node parasitic capacitor as an analog memory. Moreover, there is no significant sacrificing of any other CIS characteristics. In the fabricated test sensor, we could achieve the extended dynamic range by more than 42dB.