SESSION 6 – TAPA III
Data Converter Techniques

Thursday, June 15, 1:30 p.m.
Chairpersons: K. Gulati, BitWave Semiconductor
M. Ito, Renesas Technology Corp.

6.1 – 1:30 p.m.
A 0.5-V 1-Msample/s 60-dB SNDR Track-and-Hold Circuit, S. Chatterjee, P. Kinget, Columbia University, New York, NY

A 0.5V 1Msps track-and-hold (T/H) circuit with a 60dB SNDR is presented. The fully-differential circuit is implemented in a 0.25µm CMOS technology, with standard 0.6V VT devices, and uses true low voltage design techniques i.e. with no clock and no voltage boosting.

6.2 – 1:55 p.m.
A 12-bit 32 µW Ratio-Independent Algorithmic ADC, J.A.M. Järvinen, M. Saukoski, K. Halonen, Helsinki University of Technology, Espoo, Finland

This paper describes a ratio-independent algorithmic ADC architecture that requires a single differential amplifier and a comparator. The prototype 12-bit, 41.67 kS/s ADC with an active die area of 0.055 mm^2 is implemented in a 0.13 um CMOS. The power dissipation is minimized using a dynamically biased operational amplifier. With a 32 uW power dissipation, the ADC achieves 80 dB SFDR and 60 dB SNDR, resulting in a power FOM of 0.9 pJ/conversion.

6.3 – 2:20 p.m.
A 10MS/s 11-b 0.19mm^2 Algorithmic ADC with Improved Clocking, M.G. Kim, P.K. Hanumolu, U.-K. Moon, Oregon State University, Corvallis, OR

A 10Ms/s 11-b algorithmic ADC with an active area of 0.19mm^2 is presented. Using an improved clocking scheme, this design overcomes the speed limit of algorithmic ADCs. The proposed ADC employs amplifier sharing, DC offset ancellation, and input memory effect suppression to reduce area and power, and achieve high linearity. The ADC implemented in a 0.13um thick gate-oxide CMOS process achieves 69dB SFDR, 58dB SNR, and 56dB SNDR, while consuming 3.5mA from 3V supply.

6.4 – 2:45 p.m.
A 14-b 150 MS/s CMOS DAC with Digital Background Calibration, H.-H. Chen, J. Lee*, J. Weiner*, Y.-K. Chen*, J.-T. Chen, National Tsing Hua University, Hsinchu, Taiwan, *Lucent Technologies, Murray Hill, NJ

A 14-b 150MS/s current-steering DAC with background calibration technique is demonstrated. Digital background calibration loop trims the static performance less than +/- 0.55 LSB. The DAC achieves maximum SFDR of 81dB at 1.6MHz and 67dB at 48.75MHz for sampling rate of 150MS/s. The DAC is implemented in a 0.35 um CMOS process and active area is a 2.4x1.2 mm^2.