SESSION 7 – IOLANI I-IV
Real World Interfaces

Thursday, June 15, 1:30 p.m.
Chairpersons: T. Blalock, University of Virginia
M. Ikeda, University Tokyo

7.1 – 1:30 p.m.
A 0.8V, 88dB Dual-Channel Audio ΔΣ DAC with Headphone Driver, Q. Meng, K. Lee, T. Sugimoto*, K. Hamashita*, K. Takasuka*, S. Takeuchi*, U.-K. Moon, G.C. Temes, Oregon State University, Corvallis, OR, *Asahi Kasei Microsystems, Atsugi, Japan

A 0.8V 3rd-order ΔΣ DAC with headphone driver is presented. The circuit requires only one opamp per channel, shared by the internal DAC, the FIR and 2nd-order Sallen-Key low-pass filter, as well as by the headphone driver. The prototype IC implemented in a 0.35µm CMOS process achieved 88dB dynamic range (DR), while consuming 2.6mW from a 0.8V supply.

7.2 – 1:55 p.m.
A 0.9-V 96-µW Digital Hearing Aid Chip with Heterogeneous ΣΔ DAC, S. Kim, N. Cho, S.-J. Song, D. Kim, K. Kim, H.-J. Yoo, Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

A full chip implementation of a low-power digital hearing aid is reported. It is composed of preamplifier, Σ-Δ ADC, DSP and Σ-Δ DAC with low-power technique. The hardwired DSP has 6 parameters to reduce power consumption with high flexibility. The Σ-Δ DAC adopts heterogeneous frequency to reduce power consumption further. The proposed digital hearing aid chip achieves 79-dB peak SNR and dissipates 96-µW from a single 0.9-V supply. The core area is 2.7-mm^2 in a 0.18-µm standard CMOS technology.

7.3 – 2:20 p.m.
An Analog Frontend Chip for a MEMS-based Parallel Scanning-Probe Data-Storage System, C. Hagleitner, T. Bonaccio*, A. Pantazi, A. Sebastian, E. Eleftheriou, IBM Zurich Research Laboratory, Runschlikon, Switzerland, *IBM Systems and Technology Group, Essex Junction, VT

We present a 32-channel analog frontend chip for a parallel scanning-probe data-storage system ("millipede"-project). The chip includes all circuitry required to control the thermomechanical write-process that forms nanoscale indentations in a polymer surface. The on-chip read-channel circuitry is able to reliably detect the tiny signal-current obtained with the thermoelectrical read-process in the presence of a 1000 times larger bias current.

7.4 – 2:45 p.m.
A 1mW Dual-Chopper Amplifier for a 50-µg/√Hz Monolithic CMOS-MEMS Capacitive Accelerometer, D. Fang, H. Qu, H. Xie, University of Florida, Gainesville, FL

This paper reports a novel dual-chopper amplifier (DCA) for CMOS-MEMS capacitive accelerometers. A DCA prototype integrated with a single-axis accelerometer has been fabricated using TSMC 0.35 µm CMOS process. The DCA achieves a 16 nV/√Hz input-referred noise at 20 Hz with a power dissipation of only 1 mW. The measured accelerometer noise floor is 50 µg/√Hz down to 5 Hz.