SESSION 8 – TAPA II
On-Chip Environment and
Process Monitoring

Thursday, June 15, 3:25 p.m.
Chairpersons: V. De, Intel Corp.
H. Kabuo, Matsushita Electric Industrial Co., Ltd.

8.1 – 3:25 p.m.

A 1-ps Resolution On-chip Sampling Oscilloscope With 64:1 Tunable Sampling Range Based on Ramp Waveform Division Scheme, K. Inagaki, D.D. Antono, M. Takamiya, S. Kumashiro*, T. Sakurai, University of Tokyo, Tokyo, Japan, *Semiconductor Technology Academic Research Center, Shin-Yokohama, Japan

An on-chip sampling oscilloscope with 1ps timing resolution is realized in 90nm CMOS process based on a proposed ramp waveform division scheme for precise signal integrity and power-line integrity measurement. The resolution in time is variable from 1ps to 64ps in 64 steps. A novel on-chip inductance measurement procedure is also proposed.

8.2 – 3:50 p.m.

In-situ Measurement of Supply-Noise Maps with Millivolt Accuracy and Nanosecond-Order Time Resolution, Y. Kanno, Y. Kondoh, T. Irita*, K. Hirose*, R. Mori*, Y. Yasu*, S. Komatsu, H. Mizuno, Hitachi Ltd, Tokyo, Japan, *Renesas Technology Corp., Tokyo, Japan

An in-situ measurement scheme for supply-noise maps under running applications in product-level LSIs was developed. This scheme was used to successfully measure 69-mV local supply noise with 5-ns time resolution in a 3G cellular phone processor. It will thus help in designing power-supply networks and visibly verifying the quality of a power supply.

8.3 – 4:15 p.m.

Daisy Chain for Power Reduction in Inductive-Coupling CMOS Link, M. Inoue[1], N. Miura[1], K. Niitsu[1], Y. Nakagawa[2], M. Tago[2], M. Fukaishi[2], T. Sakurai[3], T. Kuroda[1,4], [1]Keio University, Japan, [2]NEC Corp., Japan, [3]University of Tokyo, Tokyo, Japan, [4]CREST/JST, Japan

This paper discusses a daisy chain of current-drive transmitters in inductive-coupling CMOS links. Current is reused by multiple transmitters. 8 transceivers are arranged with a pitch of 20um in 0.18um CMOS. Transmit power is saved by 35% without sacrificing data rate (1Gb/s/ch) and BER (<10-12) by having 4 transmitters daisy chained.

8.4 – 4:40 p.m.

A Test Structure for Characterizing Local Device Mismatches, K. Agarwal, F. Liu, C. McDowell, S. Nassif, K. Nowka, M. Palmer, D. Acharyya, J. Plusquellic, IBM Research, Austin, TX

We present a test structure for statistical characterization of local device mismatches. The structure contains densely populated SRAM devices arranged in an addressable manner. Measurements on a testchip fabricated in an advanced 65 nm process show little spatial correlation. We vary the nominal threshold voltage of the devices by changing the threshold-adjust implantations and observe that the ratio of standard deviation to mean gets worse with threshold scaling. The large variations observed in the extracted threshold voltage statistics indicate that the random dopant fluctuation is the likely reason behind mismatch in the adjacent devices.

8.5 – 5:05 p.m.

Impact of Layout on 90nm CMOS Process Parameter Fluctuations, L.-T. Pang, B. Nikolic, University of California, Berkeley, CA

A test chip has been built to study the effects of layout on the delay and leakage of digital circuits in 90nm CMOS. The delay is characterized through the spread of ring oscillator frequencies and the transistor leakage is measured by using an on-chip ADC.