SESSION 9 – TAPA III
Serial Link Transceivers

Thursday, June 15, 3:25 p.m .
Chairpersons: K. Yang, University of California, Los Angeles
K. Kobayashi, Kyoto University

9.1 – 3:25 p.m.
A Wide Tracking Range 0.2-4Gbps Clock and Data Recovery Circuit, P.K. Hanumolu, G.-Y. Wei*, U.-K. Moon, Oregon State University, Corvallis, OR, *Harvard University, Cambridge, MA

A hybrid analog and digital quarter-rate clock and data recovery circuit employs a second-order digital loop filter with delta-sigma truncation to achieve sub-ps phase resolution and better than 2ppm frequency resolution. A test chip fabricated in a 0.18µm CMOS process achieves BER $< 10^{\{-12\}}$ and consumes 14mW power while operating at 2Gbps. The tracking range is greater than ±5000ppm and ±2500ppm at 10kHz and 20kHz modulation frequencies respectively, thus, making this CDR suitable for systems with spread spectrum clocking.

9.2 – 3:50 p.m.
PLL On-Chip Jitter Measurement: Analysis and Design, S.D. Vamvakos, V. Stojanovic*, J.L. Zerbe**, C.W. Werner**, D. Draper**, B. Nikolic, University of California, Berkeley, CA, *Massachusetts Institute of Technology, Cambridge, MA, **Rambus Inc., Los Altos, CA

Analysis of on-chip jitter measurements based on the dead-zone method reveals potentially large errors in the jitter variance estimate, when the jitter distribution is changing or not known a priori. To overcome this, a more accurate variance estimation method is proposed and experimentally verified. The residual error, caused by the correlated noise between the PLL and the measurement circuit, is fully characterized and circuit topologies are proposed to mitigate this type of error.

9.3 – 4:15 p.m.
A Sub-picosecond Resolution 0.5-1.5GHz Digital-to-Phase Converter, P.K. Hanumolu, V. Kratyuk, G.-Y. Wei*, U.-K. Moon, Oregon State University, Corvallis, OR, *Harvard University, Cambridge, MA

A digital-to-phase converter operating from 0.5-1.5GHz employs oversampling, noise shaping and DLL phase filtering to achieve sub-ps resolution independent of the operating frequency. Test chip fabricated in a 0.13µm CMOS process achieves a DNL below ±100fs and ±pm12ps INL and consumes 15mW while operating at 1GHz.

9.4 – 4:40 p.m.
A Low Power 4.2Gb/s/pin Parallel Link Using Three-Level Differential Encoding, S. Zogopoulos, W. Namgoong, University of Southern California, CA

A three-level encoding scheme is proposed to reduce power and increase the data rate in high-speed parallel transceiver system. The proposed encoding scheme transmits 3-bit of information via four pins to overcome the two major problems in single-ended links – reference ambiguity and power line fluctuations – while minimizing power consumption and the effects of inter-symbol interference (ISI). The proposed parallel link, which is designed in 0.18um CMOS process, achieves a data rate of 4.2Gb/s/pin while dissipating 17.1mW/Gb/s.

9.5 – 5:05 p.m.
Power/Performance/Channel Length Tradeoffs in 1.6 to 9.6Gbps I/O Links in 90nm CMOS for Server, Desktop, and Mobile Applications, E. Yeung, K. Canagasaby, A. Tripathi, S. Chaudhuri, P. Meier, J. Prijic, V. Joshi, M. Mazumder, S. Dabral, Intel Corp., Santa Clara, CA

Performance and power of 1.6 to 9.6Gbps server, desktop, and mobile I/O links in a 1.2V 90nm CMOS test chip implementing equalized voltage-mode and current-mode drivers, TX and RX equalizers, self-biased ring oscillator and LC PLLs, and different RX clocking schemes are compared. The novel combination of voltage-mode driver (equalized or unequalized) and RX equalizer delivers the lowest power (12.1mW/Gbps at 7.2Gbps), offering a low-power option for short-distance links.