2006 VLSI Circuits Short Course

This year the Circuits Short Course is comprised of two programs, Analog and Digital. The cost of the short course includes both programs and attendees will receive one book for both programs. Attendees will be able to move back and forth between the two programs.

Analog Short Course Program

Data Converter Design for Embedded Systems

Honolulu I
Wednesday, June 14, 8:10 a.m.

Organizers/Chairs: Katsu Nakamura, Analog Devices
Hiroshi Yamazaki, Fujitsu Labs

8:10 a.m.	**Introduction** K. Nakamura, Analog Devices
8:15 a.m.	**Introduction to Embedded Data Converters** A. Matsuzawa, Tokyo Institute of Technology
9:25 a.m.	**High-Speed Analog-to-Digital Converters** M. Pelgrom, Philips Research
10:35 a.m.	**Break**
10:50 a.m.	**Precision Analog-to-Digital Converters** C. Lyden, Analog Devices
12:00 p.m.	**Lunch**
1:30 p.m.	**High-Speed and Precision Digital-to-Analog Converters** M. Hotta, Musashi Institute of Technology
2:40 p.m.	**Break**
2:55 p.m.	**Practical Considerations for Embedded Data Converters** J. Wieser, National Semiconductor
4:05 p.m.	**Design for Testability of Data Converter Circuits in Embedded Systems** G. Roberts, McGill University
5:15 p.m.	**Conclusion** H. Yamazaki, Fujitsu Labs

Digital Short Course Program

Designing for Paradigm Shifts in Microprocessors and Networking

Honolulu II
Wednesday, June 14, 8:10 a.m.

Organizers/Chairs: Steven Butler, AMD
Hideyuki Kabuo, Panasonic

8:10 a.m.	**Introduction** S. Butler, Advanced Micro Devices
8:15 a.m.	**Technology** M. Hane, NEC
9:25 a.m.	**Architecture** C. Moore, Advanced Micro Devices
10:35 a.m.	**Break**
10:50 a.m.	**SOC Integration** P, Rickert, Texas Instruments
12:00 p.m.	**Lunch**
1:30 p.m.	**Security** A. Satoh, IBM Japan
2:40 p.m.	**Break**
2:55 p.m.	**Sensor Networking** K. Suzuki, Hitachi
4:05 p.m.	**Power-Constrained Performance** S. Rusu, Intel
5:15 p.m.	**Conclusion** H. Kabuo, Panasonic

Welcome to the 2006 Symposium on VLSI Circuits

You are cordially invited to attend the 2006 Symposium on VLSI Circuits, to be held on June 15-17th, 2006, at the Hilton Hawaiian Village in Honolulu, Hawaii. Following the tradition of the last several years, the Symposium on VLSI Circuits will follow the Symposium on VLSI Technology at the same location.

Starting in 1987, this year marks the 20th annual Symposium on VLSI Circuits. The Symposium has established itself as a major international forum for presenting and exchanging important ideas and new developments in VLSI circuit design. The scope of the conference includes new concepts in VLSI, novel Memory technologies, Analog Circuits, Analog/Digital Conversion, Digital Processing, Static and Dynamic Memory, Signal Processing, I/O and Communication circuits. Contributions to the Symposium come from both industry and academia, from around the world.

New for this year, preceding the Symposium on June 14th, two all-day Short Courses on VLSI circuits will be held. For one registration fee, participants can attend either parallel course. The first focusing on new challenges facing digital designers titled; “Designing for Paradigm Shifts in Microprocessors and Networking”, the other choice focuses on the increasing challenges of Analog and Digital conversion in advanced technologies titled; “Data Converter Design for Embedded Systems”.

This year, the technical program committee reviewed 412 papers, selecting 113 outstanding papers for presentation. These papers disclose new and interesting design concepts for memory, processor, communication, analog, and signal processing circuits, and represent the leading edge of VLSI circuit design.

We have invited four distinguished speakers to describe recent advances and new challenges related to VLSI circuits, technology and applications: “High Performance Processors in a Power Limited World”, “Finger-Vein Authentication Technology and its Future”, “Analog and The Big Bang: A Universal Model for Mixed Signal VLSI Trends”, “Through Silicon Via and 3-D Wafer/Chip Stacking Technology”.

To complement the formal talks, we have arranged three evening rump sessions on interesting and provocative subjects to give you an opportunity to participate in the discussions and mix with the participants who were chosen to represent contrasting opinions on the topics. The rump sessions explore: “What will be the next embedded memory workhorse?”; “Power management: What are the device and circuit trade-offs and how will it be managed at 45nm and 32nm nodes”; “Complete integration of SoC power management - reality or mirage?”.

The rich technical content of the program will undoubtedly interest you, and we certainly hope that the Symposium will be a fruitful and enjoyable experience.

This booklet contains the advance program together with forms for the Symposium registration and hotel reservations. Please try to complete and return these forms as soon as possible. Although the on-site registration will be available at the conference, pre-registration will facilitate Symposium planning.

We look forward to meeting with you at the Symposium in Honolulu.

Stephen V. Kosonocky	Kazuo Yano
Program Chair	Program Co-Chair

SESSION I – TAPA II
Plenary Session I

Thursday, June 15, 8:00 a.m.
Chairpersons: S. Kosonocky, IBM TJ Watson Research Center
K. Yano, Hitachi, Ltd.

8:00 a.m. Welcome and Opening Remarks
B. Gieseke, AMD
T. Kuroda, Keio University

1.1 – 8:15 a.m.
The Past, Present, and Future of Data Converters and Mixed Signal ICs: a "Universal" Model, David Robertson, Analog Devices

1.2 – 9:00 a.m.
Finger-Vein Authentication Technology and Its Future, Junichi Hashimoto, Hitachi, Ltd.

9:45 a.m. Break

SESSION 2 – TAPA II
SRAM Cell Stability

Thursday, June 15, 10:00 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
T. Kawahara, Hitachi

2.1 – 10:00 a.m.
Wordline & Bitline Pulsing Schemes for Improving SRAM Cell Stability in Low-Vcc 65nm CMOS Designs, M. Khellah, Y. Ye, N.S. Kim, D. Somasekhar, G. Pandya, A. Farhang, K. Zhang, C. Webb, V. De, Intel, Hillsboro, OR

2.2 – 10:25 a.m.
A Stable SRAM Cell Design Against Simultaneously R/W Disturbed Accesses, T. Suzuki, H. Yamauchi*, Y. Yamagami, K. Satomi, H. Akamatsu, Matsushita Electric Industrial Co., Ltd., Kyoto, Japan, *Fukuoka Institute of Technology, Fukuoka, Japan

2.3 – 10:50 a.m.
A Vth-Variation-Tolerant SRAM with 0.3-V Minimum Operation Voltage for Memory-Rich SoC under DVS Environment, Y. Morita, H. Fujiwara*, H. Noguchi*, K. Kawakami*, J. Miyakoshi*, S. Mikami, K. Nii*, H. Kawaguchi*, M. Yoshimoto*, Kanazawa University, *Kobe University, Kobe, Japan

2.4 – 11:15 a.m.
An SRAM Design in 65nm and 45nm Technology Nodes Featuring Read and Write-Assist Circuits to Expand Operating Voltage, H. Pilo, J. Barwin, G. Braceras, C. Browning, S. Burns, J. Gabric, S. Lamphier, M. Miller, A. Roberts, F. Towler, IBM Systems and Technology Group, Essex Junction, VT

2.5 – 11:40 a.m.
A 65 nm SoC Embedded 6T-SRAM Design for Manufacturing with Read and Write Cell Stabilizing Circuits, S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka*, Y. Oda*, M. Igarashi, M. Takeuchi, H. Kawashima, H. Makino, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, K. Ishibashi, H. Shinohara, Renesas Technology Corp., Hyogo, Japan, *Renesas Design Corp., Hyogo, Japan

12:05 p.m. Lunch

SESSION 3 – TAPA III
Image Sensors

Thursday, June 15, 10:00 a.m.
Chairpersons: T. Blalock, University of Virginia
S. Sugawa, Tohoku University

3.1 – 10:00 a.m.
WITHDRAWN –

3.2 – 10:25 a.m.
A 76 x 77mm^2, 16.85 Million Pixel CMOS APS Image Sensor, S.U. Ay, E.R. Fossum*, Micron Technology Inc., Pasadena, CA, *University of Southern California, Los Angeles, CA

3.3 – 10:50 a.m.
A 3500fps High-Speed CMOS Image Sensor with 12b Column-Parallel Cyclic A/D Converters, M. Furuta, T. Inoue*, Y. Nishikawa, S. Kawahito, Shizuoka Univ., Hamammatsu, Japan, *Photron Ltd., Tokyo, Japan

3.4 – 11:15 a.m.
A 0.88nW/pixel, 99.6 dB Linear-Dynamic-Range Fully-Digital Image Sensor Employing a Pixel-Level Sigma-Delta ADC, Z. Ignjatovic, M.F. Bocko, University of Rochester, Rochester, NY

3.5 – 11:40 a.m.
A High Dynamic Range CMOS Image Sensor with In-Pixel Floating-Node Analog Memory for Pixel Level Integration Time Control, S.-W. Han, S.-J. Kim, J.-H. Choi*, C.-K. Kim, E. Yoon*, KAIST, Daejeon, Korea, *University of Minnesota, Minneapolis, MN

12:05 p.m. Lunch

SESSION 4 – IOLANI I-IV
Clock Generation for High Speed Transceivers

Thursday, June 15, 10:00 a.m.
Chairpersons: G. Taylor, Intel Corp.
M. Mizuno, NEC Corp.

4.1 – 10:00 a.m.
A 1.2V 37-38.5GHz 8-Phase Clock Generator in 0.13um CMOS Technology, C. Lee, L.-C. Chou, S.-I. Liu, C.-L. Ko*, Y.-Z. Juang*, C.-F. Chiu*, National Taiwan University, Taipei, Taiwan, *National Applied Research Lab, Hsinchu, Taiwan

4.2 – 10:25 a.m.
A Low-Jitter PLL and Repeaterless Clock Distribution Network for a 20Gb/s Link, F. O'Mahony, M. Mansuri, B. Casper, J.E. Jaussi, R. Mooney, Intel Corp., Hillsboro, OR

4.3 – 10:50 a.m.
A Digital PLL with a Stochastic Time-to-Digital Converter, V. Kratyuk, P.K. Hanumolu, K. Ok, K. Mayaram, U.-K. Moon, Oregon State University, Corvallis, OR

4.4 – 11:15 a.m.
An Ultra-Wide Range Digitally Adaptive Control Phase Locked Loop with New 3-Phase Switched Capacitor Loop Filter, S. Dosho, N. Yanagisawa, K. Sogawa, Y. Yamada, T. Morie, Matsushita Electric Industrial Co. Ltd., Osaka, Japan

4.5 – 11:40 a.m.
A Multiphase Delay-Locked Loop for 0.125-2Gbps 0.18µm CMOS Transmitter, Y. Moon, D. Shim, Silicon Image Inc., Sunnyvale, CA

12:05 p.m. Lunch

SESSION 5 – TAPA II
RF Blocks for Tuners and Sensor Networks

Thursday, June 15, 1:30 p.m.
Chairpersons: F. Dai, Auburn University
K. Agawa, Toshiba Corp.

5.1 – 1:30 p.m.
A Fully-Integrated 0.13µm CMOS Low-IF DBS Satellite Tuner, A. Maxim, R. Poorfard, R. Johnson, P. Crawley, J. Kao, Z. Dong, M. Chennam, T. Nutt, D. Trager, Silicon Laboratories Inc., Austin, TX

5.2 – 1:55 p.m.
A 184mW Fully Integrated DVB-H Tuner Chip with Distortion Compensated Variable Gain LNA, H. Kawamura, T. Fujiwara, K. Kagoshima, S. Kawama, H. Kijima, M. Koutani, S. Toyoyama, K. Sakuno, K. Iizuka, Sharp Corp., Nara, Japan

5.3 – 2:20 p.m.
9.75/10.6GHz SiGe PLL for LNB Satellite Front-Ends Using Half-Rate Oscillators, A. Maxim, M. Gheorghe, C. Turinici, Integrated Products, Austin, TX

5.4 – 2:45 p.m.
A 46% Efficient 0.8dBm Transmitter for Wireless Sensor Networks, Y.H. Chee, A.M. Niknejad, J. Rabaey, University of California, Berkeley, CA

3:10 p.m. Break

SESSION 6 – TAPA III
Data Converter Techniques

Thursday, June 15, 1:30 p.m.
Chairpersons: K. Gulati, BitWave Semiconductor
M. Ito, Renesas Technology Corp.

6.1 – 1:30 p.m.
A 0.5-V 1-Msample/s 60-dB SNDR Track-and-Hold Circuit, S. Chatterjee, P. Kinget, Columbia University, New York, NY

6.2 – 1:55 p.m.
A 12-bit 32 µW Ratio-Independent Algorithmic ADC, J.A.M. Järvinen, M. Saukoski, K. Halonen, Helsinki University of Technology, Espoo, Finland

6.3 – 2:20 p.m.
A 10MS/s 11-b 0.19mm^2 Algorithmic ADC with Improved Clocking, M.G. Kim, P.K. Hanumolu, U.-K. Moon, Oregon State University, Corvallis, OR

6.4 – 2:45 p.m.
A 14-b 150 MS/s CMOS DAC with Digital Background Calibration, H.-H. Chen, J. Lee*, J. Weiner*, Y.-K. Chen*, J.-T. Chen, National Tsing Hua University, Hsinchu, Taiwan, *Lucent Technologies, Murray Hill, NJ

3:10 p.m. Break

SESSION 7 – IOLANI I-IV
Real World Interfaces

Thursday, June 15, 1:30 p.m.
Chairpersons: T. Blalock, University of Virginia
M. Ikeda, University Tokyo

7.1 – 1:30 p.m.
A 0.8V, 88dB Dual-Channel Audio ΔΣ DAC with Headphone Driver, Q. Meng, K. Lee, T. Sugimoto*, K. Hamashita*, K. Takasuka*, S. Takeuchi*, U.-K. Moon, G.C. Temes, Oregon State University, Corvallis, OR, *Asahi Kasei Microsystems, Atsugi, Japan

7.2 – 1:55 p.m.
A 0.9-V 96-µW Digital Hearing Aid Chip with Heterogeneous ΣΔ DAC, S. Kim, N. Cho, S.-J. Song, D. Kim, K. Kim, H.-J. Yoo, Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea

7.3 – 2:20 p.m.
An Analog Frontend Chip for a MEMS-based Parallel Scanning-Probe Data-Storage System, C. Hagleitner, T. Bonaccio*, A. Pantazi, A. Sebastian, E. Eleftheriou, IBM Zurich Research Laboratory, Runschlikon, Switzerland, *IBM Systems and Technology Group, Essex Junction, VT

7.4 – 2:45 p.m.
A 1mW Dual-Chopper Amplifier for a 50-µg/√Hz Monolithic CMOS-MEMS Capacitive Accelerometer, D. Fang, H. Qu, H. Xie, University of Florida, Gainesville, FL

3:10 p.m. Break

SESSION 8 – TAPA II
On-Chip Environment and Process Monitoring

Thursday, June 15, 3:25 p.m.
Chairpersons: V. De, Intel Corp.
H. Kabuo, Matsushita Electric Industrial Co., Ltd.

8.1 – 3:25 p.m.
A 1-ps Resolution On-chip Sampling Oscilloscope With 64:1 Tunable Sampling Range Based on Ramp Waveform Division Scheme, K. Inagaki, D.D. Antono, M. Takamiya, S. Kumashiro*, T. Sakurai, University of Tokyo, Tokyo, Japan, *Semiconductor Technology Academic Research Center, Shin-Yokohama, Japan

8.2 – 3:50 p.m.
In-situ Measurement of Supply-Noise Maps with Millivolt Accuracy and Nanosecond-Order Time Resolution, Y. Kanno, Y. Kondoh, T. Irita*, K. Hirose*, R. Mori*, Y. Yasu*, S. Komatsu, H. Mizuno, Hitachi Ltd, Tokyo, Japan, *Renesas Technology Corp., Tokyo, Japan

8.3 – 4:15 p.m.
Daisy Chain for Power Reduction in Inductive-Coupling CMOS Link, M. Inoue[1], N. Miura[1], K. Niitsu[1], Y. Nakagawa[2], M. Tago[2], M. Fukaishi[2], T. Sakurai[3], T. Kuroda[1,4], [1]Keio University, Japan, [2]NEC Corp., Japan, [3]University of Tokyo, Tokyo, Japan, [4]CREST/JST, Japan

8.4 – 4:40 p.m.
A Test Structure for Characterizing Local Device Mismatches, K. Agarwal, F. Liu, C. McDowell, S. Nassif, K. Nowka, M. Palmer, D. Acharyya, J. Plusquellic, IBM Research, Austin, TX

8.5 – 5:05 p.m.
Impact of Layout on 90nm CMOS Process Parameter Fluctuations, L.-T. Pang, B. Nikolic, University of California, Berkeley, CA

SESSION 9 – TAPA III
Serial Link Transceivers

Thursday, June 15, 3:25 p.m .
Chairpersons: K. Yang, University of California, Los Angeles
K. Kobayashi, Kyoto University

9.1 – 3:25 p.m.
A Wide Tracking Range 0.2-4Gbps Clock and Data Recovery Circuit, P.K. Hanumolu, G.-Y. Wei*, U.-K. Moon, Oregon State University, Corvallis, OR, *Harvard University, Cambridge, MA

9.2 – 3:50 p.m.
PLL On-Chip Jitter Measurement: Analysis and Design, S.D. Vamvakos, V. Stojanovic*, J.L. Zerbe**, C.W. Werner**, D. Draper**, B. Nikolic, University of California, Berkeley, CA, *Massachusetts Institute of Technology, Cambridge, MA, **Rambus Inc., Los Altos, CA

9.3 – 4:15 p.m.
A Sub-picosecond Resolution 0.5-1.5GHz Digital-to-Phase Converter, P.K. Hanumolu, V. Kratyuk, G.-Y. Wei*, U.-K. Moon, Oregon State University, Corvallis, OR, *Harvard University, Cambridge, MA

9.4 – 4:40 p.m.
A Low Power 4.2Gb/s/pin Parallel Link Using Three-Level Differential Encoding, S. Zogopoulos, W. Namgoong, University of Southern California, CA

9.5 – 5:05 p.m.
Power/Performance/Channel Length Tradeoffs in 1.6 to 9.6Gbps I/O Links in 90nm CMOS for Server, Desktop, and Mobile Applications, E. Yeung, K. Canagasaby, A. Tripathi, S. Chaudhuri, P. Meier, J. Prijic, V. Joshi, M. Mazumder, S. Dabral, Intel Corp., Santa Clara, CA

SESSION 10 – IOLANI I-IV
Analog Techniques

Thursday, June 15, 3:25 p.m.
Chairpersons: A. Abidi, University of California, Los Angeles
K. Agawa, Toshiba Corp.

10.1 – 3:25 p.m.
A 300 nW, 12 ppm/°C Voltage Reference in a Digital 0.35 µm CMOS Process, G. De Vita, G. Iannaccone, P. Andreani*, Universitá di Pisa, Pisa, Italy, *Technical University of Denmark, Lyngby, Denmark

10.2 – 3:50 p.m.
A 1.4-V Supply CMOS Fractional Bandgap Reference, R.T. Perry, S.H. Lewis, A.P. Brokaw*, T.R. Viswanathan**, University of California, Davis, CA, *Analog Devices Inc., **University of Texas, Dallas, TX

10.3 – 4:15 p.m.
An Integrated 1.8V to 3.3V Regulated Voltage Doubler using Active Diodes and Dual-Loop Voltage Follower for Switch-Capacitive Load, Y.-H. Lam, W.-H. Ki, C.-Y. Tsui, Hong Kong University of Science and Technology, Hong Kong, China

10.4 – 4:40 p.m.
0.9-V Rail-to-Rail Operational Amplifiers with Adaptive Threshold Voltage Control, T. Adachi, K. Takasuka, Asahi Kasei Microsystems, Kanagawa, Japan

JOINT TECHNOLOGY/CIRCUITS
RUMP SESSION
Wednesday, June 14
8:00 p.m – 10:00 p.m.

Joint Rump Session Organizers:
C.K. Ken Yang, UCLA
K. Kobayashi, Kyoto Univ.
S. Sharifzadeh, Cypress
Y. Renichi, Hitachi

RJ1 Power Management: What are the Device and Circuit Trade-offs. How Will it be Managed at 45nm and 32nm Nodes?
Tapa I
Organizers:

Circuits	**Technology**
K. Nowka, IBM	H. Puchner, Cypress
Y.Oowaki, Toshiba	T. Ipposhi, Renesas

Moderator: T. Skotnicki, ST Microelectronics

Power management has historically focused on low standby and operating power for mobile devices to increase the battery time. In today's designs, it is increasingly important to optimize power for all electronic applications. Data centers can consume the power of small cities. Previous efforts for power reduction have been focusing on technology as well as design options to reduce standby power. However, it is not clear which of the options will be available in future designs and what other limitations will arise from these reduction techniques. The discussion panel is a compilation of design and process experts and will present view on power management for the 45-nm and 32-nm

technology nodes. The panelists will present classical power reduction techniques such as gate leakage, sleeper transistors, cascading, fundamental improvements in leakage performance due to new device architectures. Various techniques will be debated on their merits for high-power vs low-power products or memory-intensive vs logic-dominated designs and technologies.

Panelists:

Y. Urakawa, Toshiba
U. Ko, Texas Instruments
D. Frank, IBM
R. Kumar, Intel Corp
Y. Yamagata, NEC
D. Ditzel, Transmeta

CIRCUITS RUMP SESSION
Thursday, June 15
8:00 p.m. – 10:00 p.m.

Organizers: C.K. Ken Yang, UCLA
K. Kobayashi, Kyoto University

R1: Complete Integration of SoC Power Management - Reality or Mirage?
Honolulu I
Organizers/Moderators: K. Gulati, BitWave Semi.
M. Hiraki, Renesas Technology

SoCs often employ a diverse set of circuits – RF, analog, digital, I/O, memory – each with a different set of demands on the supply voltage level, noise, loading and its adaptability to chip performance. Integrating supply converters improves form-factor, system yield, bill-of-materials and efficiency. Yet it is not clear how bulky inductors and large capacitors can be integrated cost effectively. How should these converters be modified to enable integration? How do battery voltage level and process technology influence the selection of converter architecture? Can switching regulators be used for powering sensitive RF and analog circuits? How will next generation energy sources influence power management? This panel will consider all of these issues and more in the context of SoCs for future portable devices.

Panelists:

S. Dosho, Matsushita
Y. Kanno, Hitachi
T. Karnik, Intel
K. Kunz, Texas Instruments
B. Miwa, Maxim Integrated
G. Rincón-Mora, Georgia Inst. of Tech

R2: What Will be the Next Embedded Memory Workhorse?
Honolulu II
Organizers: S. Natarajan, Emerging Memory Technologies, Inc.
K. Noda, N Score

Moderator: S. Natarajan, Emerging Memory Technologies, Inc.

6T-SRAM technology has been the dominant embedded memory of choice primarily due to its high performance, excellent CMOS compatibility, and manufacturing robustness. At 45nm and 32nm technology nodes, because of ever-increasing device variability and the need for transistor voltage

down-scaling, the stability of 6T-SRAM cell becomes a significant issue that likely requires significant cell area penalty to overcome.

Alternative embedded memory technologies to 6T-SRAM have been the subject of research and development for many years. Few of these alternative technologies, however, have proven to be viable or have been able to match 6T-SRAM in high-performance applications. Thyristor-based memory (T-RAM) is emerging as an attractive embedded memory solution for 45nm and beyond, especially with the increasing adoption of process/device technologies such as SOI and FinFET in deep nano-scale CMOS.

T-RAM technology offers 6T-SRAM performance and functionality at more than twice the macro density, a simple process addition into a baseline SOI CMOS technology that involves extra implant steps only, and a straight-line layout that greatly simplifies lithography.

Panelists:

P. Rickert, TI
H. Pilo, IBM
T. Furuyama, Toshiba
S. Chung, TSMC
S. Rusu, Intel Corp.
F. Nemati, T-RAM Inc

SESSION 11 – TAPA II
Plenary Session II

Friday, June 16, 8:00 a.m.
Chairpersons: S. Kosonocky, IBM TJ Watson Research Center
K. Yano, Hitachi, Ltd.

11.1 – 8:00 a.m.
Through Silicon Via and 3-D Wafer/Chip Stacking Technology, Kenji Takahashi, Toshiba Corp.

11.2 – 8:45 a.m.
High Performance Processors in a Power Limited World, Sam Naffziger

9:30 a.m. Break

SESSION 12 – TAPA I
Clock Generation and Distribution

Friday, June 16, 8:00 a.m.
Chairpersons: J. Farrell, AMD
M. Nagata, Kobe University

12.1 – 9:45 a.m.
17GHz Fine Grid Clock Distribution with Uniform-Amplitude Standing-Wave Oscillator, M. Sasaki, M. Shiozaki, A. Mori, A. Iwata, H. Ikeda*, Hiroshima University, Hiroshima, Japan, *Elpida Memory Inc., Kanagawa, Japan

12.2 – 10:10 a.m.
175 GMACS/mW Charge-Mode Adiabatic Mixed-Signal Array Processor, R. Karakiewicz, R. Genov, A. Abbas*, G. Cauwenberghs**, University of Toronto, Canada, *Johns Hopkins University, MD, **University of California, San Diego, CA

12.3 – 10:35 a.m.
An On-chip Calibration Technique for Reducing Supply Voltage Sensitivity in Ring Oscillators, T. Wu, K. Mayaram, U.-K. Moon, Oregon State University, Corvallis, OR

12.4 – 11:00 a.m.
A 0.004mm^2 Portable Multiphase Clock Generator Tile for 1.2GHz RISC Microprocessor, I. Jung, G. Jung*, J. Song, M.-Y. Kim, J. Park*, S.B. Park*, C. Kim, Korea University, Seoul, Korea, *Samsung Electronics Corp., Yongin, Korea

12.5 – 11:25 a.m.
A Duty-Cycle Correction Circuit for High-Frequency Clocks, K. Agarwal, R. Montoye, IBM, Austin, TX

11:55 a.m. Lunch

SESSION 13 – TAPA II
Non-Volatile Memory Architecture and Circuits

Friday, June 16, 9:45 a.m.
Chairpersons: H. Pon, Intel Corp.
T. Sekiguchi, Hitachi, Ltd.

13.1 – 9:45 a.m.
MRAM Cell Technology for Over 500MHz SoC, N. Sakimura, T. Sugibayashi, T. Honda, H. Honjo, S. Saito, T. Suzuki, N. Ishiwata, S. Tahara, NEC Corp., Kanagawa, Japan

13.2 – 10:10 a.m.
A Non-Volatile 2Mbit CBRAM Memory Core Featuring Advanced Read and Program Control, H. Hönigschmid, M. Angerbauer, S. Dietrich, M. Dimitrova, D. Gogl, C. Liaw, M. Markert, R. Symanczyk, L. Altimime, S. Bournat*, G. Müller, Infineon Technologies, Neubiberg, Germany, *Altis Semiconductor, Corbeil Essonnes, France

13.3 – 10:35 a.m.
The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories, H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi*, K. Tokami*, S. Kamohara*, O. Tsuchiya*, Hitachi Ltd., Tokyo, Japan, *Renesas Technology Corp., Tokyo, Japan

13.4 – 11:00 a.m.
Design of 90nm 1Gb ORNAND™ Flash Memory with MirrorBit™ Technology, T.H. Kuo, N. Yang, N. Leong, E. Wang, F. Lai, A. Lee, H. Chen, S. Chandra, Y. Wu, T. Akaogi, A. Melik-Martirosian, A. Pourkeramati, J. Thomas, M. VanBuskirk, Spansion LLC, Sunnyvale, CA

13.5 – 11:25 a.m.
A Novel Program and Read Architecture for Contact-Less Virtual Ground NOR Flash Memory for High Density Application, N. Ito, Y. Yamauchi, N. Ueda, K. Yamamoto, Y. Sugita, T. Mineyama, A. Ishihama, K. Moritani, Sharp Corp., Nara, Japan

11:55 a.m. Lunch

SESSION 14 – TAPA III
Serial Receivers

Friday, June 16, 9:45 a.m.
Chairpersons: K. Yang, University of California, Los Angeles
M. Mizuno, NEC Corp.

14.1 – 9:45 a.m.
A Fully Integrated 10Gbps Receiver with Adaptive Optical Dispersion Equalizer in 0.13µm CMOS, A. Momtaz, D. Chung, N. Kocaman, M. Caresosa, J. Cao, B. Zhang, I. Fujimori, Broadcom Corp., Irvine, CA

14.2 – 10:10 a.m.
A Single Chip 2.5 Gbps CMOS Burst Mode Optical Receiver, W.-Z. Chen, R.-M. Gan*, National Chiao-Tung University, Hsin-Chu, Taiwan, *Industrial Technology Research Institute, Hsin-Chu, Taiwan

14.3 – 10:35 a.m.
A 35-Gb/s Limiting Amplifier in 0.13um CMOS Technology, C. Lee, S.-I. Liu, National Taiwan University, Taipei, Taiwan

14.4 – 11:00 a.m.
A 100-Gb/s 1:2 Demultiplexer, Y. Suzuki, M. Mamada, Z. Yamazaki, NEC Corp., Kanagawa, Japan

14.5 – 11:25 a.m.
A 10 GHz Discrete-Time Analog FIR Filter, Y. Cai, G.A. De Veirman, Menara Networks, Irvine, CA

11:55 a.m. Lunch

SESSION 15 – TAPA I
SRAM Architecture and Techniques

Friday, June 16, 1:30 p.m.
Chairpersons: S. Butler, AMD
C. Kim, Samsung Electronics Co., Ltd.

15.1 – 1:30 p.m.
The 65nm 16MB On-die L3 Cache for a Dual Core Multi-Threaded Xeon® Processor, J. Chang, M. Huang, J. Shoemaker, J. Benoit, S.-L. Chen, W. Chen, S. Chiu, R. Ganesan, G. Leong, V. Lukka, S. Rusu, D. Srivastava, Intel Corp., Santa Clara, CA

15.2 – 1:55 p.m.
A SRAM Core Architecture with Adaptive Cell Bias Scheme, H.-S. Yu, N.-S. Kim, Y.-J. Son, Y.-G. Kim, H.-C. Kim, U.-R. Cho, H.-G. Byun, Samsung Electronics, Kyeonggi-Do, Korea

15.3 – 2:20 p.m.
A 65 nm Ultra-High-Density Dual-port SRAM with 0.71um^2 8T-cell for SoC, K. Nii, Y. Masuda*, M. Yabuuchi*, Y. Tsukamoto, S. Ohbayashi, S. Imaoka*, M. Igarashi, K. Tomita, N. Tsuboi, H. Makino, K. Ishibashi, H. Shinohara, Renesas Technology Corp., Hyogo, Japan, *Renesas Design Corp., Hyogo, Japan

15.4 – 2:45 p.m.
Self-Repairing SRAM for Reducing Parametric Failures in Nanoscaled Memory, S. Mukhopadhyay, K. Kim, H. Mahmoodi*, A. Datta, D. Park, K. Roy, Purdue University, West Lafayette, IN, *San Francisco State University, San Francisco, CA

3:10 p.m. Break

SESSION 16 – TAPA II
Nyquist ADC 1

Friday, June 16, 1:30 p.m.
Chairpersons: K. Nakamura, Analog Devices
H. Yamazaki, Fujitsu Laboratories Ltd.

16.1 – 1:30 p.m.
A 6-bit 800-MS/s Pipelined A/D Converter with Open-loop Amplifiers, D.-L. Shen, T.-C. Lee, National Taiwan University, Taipei, Taiwan

16.2 – 1:55 p.m.
A 1-V 100MS/s 8-bit CMOS Switched-Opamp Pipelined ADC Using Loading-Free Architecture, Y. Wu, V.S.L. Cheung, H. Luong, Hong Kong University of Science and Technology, Kowloon, Hong Kong

16.3 – 2:20 p.m.
A 7bit 800Msps 120mW Folding and Interpolation ADC Using a Mixed-Averaging Scheme, K. Makigawa, K. Ono, T. Ohkawa, K. Matsuura, M. Segami, Sony Corp., Kanagawa, Japan

16.4 – 2:45 p.m.
A 500MS/s 5b ADC in 65nm CMOS, B.P. Ginsburg, A.P. Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA

3:10 p.m. Break

SESSION 17 – TAPA III
MM-Wave

Friday, June 16, 1:30 p.m.
Chairpersons: M. Huang, Freescale Semiconductor
M. Ugajin, NTT Microsystem Integration Labs

17.1 – 1:30 p.m.
A Millimeter-Wave Schottky Diode Detector in 130-nm CMOS Technology, E. Seok, C. Cao, S. Sankaran, K.K. O, University of Florida, Gainesville, FL

17.2 – 1:55 p.m.
A 60GHz CMOS Differential Receiver Front-End Using On-Chip Transformer for 1.2 Volt Operation with Enhanced Gain and Linearity, D. Huang, R. Wong, Q. Gu, N.-Y. Wang, T.W. Ku, C. Chien*, M.-C.F. Chang, University of California, Los Angeles, CA, *SST Communications Co., Los Angeles, CA

17.3 – 2:20 p.m.
A 9.5-dB 50-GHz Matrix Distributed Amplifier in 0.18-μm CMOS, J.-C. Chien, T.-Y. Chen, L.-H. Lu, National Taiwan University, Taipei, Taiwan

17.4 – 2:45 p.m.
A 24-GHz Transmitter with an On-chip Antenna in 130-nm CMOS, C. Cao, Y. Ding, X. Yang, J.-J. Lin, A. K. Verma, J. Lin, F. Martin*, K.K. O, University of Florida, Gainesville, FL, *Motorola Labs, Fort Lauderdale, FL

3:10 p.m. Break

SESSION 18 – TAPA I
Digital Processing

Friday, June 16, 3:25 p.m.
Chairpersons: K. Nowka, IBM
M. Ikeda, University Tokyo

18.1 – 3:25 p.m.
A 0.79mm^2 29mW Real-Time Face Detection Core, Y. Hori, M. Kusaka, T. Kuroda, Keio University, Yokohama, Japan

18.2 – 3:50 p.m.
1.047GHz, 1.2V, 90nm CMOS, 2-Way VLIW DSP Core Using Saturation Anticipator Circuit, H. Suzuki, H. Takata, H. Shinohara, E. Teraoka, M. Matsuo, T. Yoshida, H. Sato, N. Honda, N. Masui, T. Shimizu, Renesas Technology Corp., Itami, Japan

18.3 – 4:15 p.m.
A 2.60pJ/Inst Subthreshold Sensor Processor for Optimal Energy Efficiency, B. Zhai, L. Nazhandali, J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, D. Blaauw, T. Austin, University of Michigan, Ann Arbor, MI

18.4 – 4:40 p.m.
A Watchdog Sensor for Assuring the Quality of Various Perishables with Subthreshold CMOS Circuits, K. Ueno, T. Hirose, T. Asai, Y. Amemiya, Hokkaido University, Hokkaido, Japan

18.5 – 5:05 p.m.
A 70GOPS, 34mW Multi-Carrier MIMO Chip in 3.5mm^2, D. Markovic, R.W. Brodersen, B. Nikolic, Univ. of California, Berkeley, CA

SESSION 19 – TAPA II
Oversampled ADCs

Friday, June 16, 3:25 p.m.
Chairpersons: K. Nakamura, Analog Devices
S. Sugawa, Tohoku University

19.1 – 3:25 p.m.
A 0.9V 92dB Double-Sampled Switched-RC ΔΣ Audio ADC, M.G. Kim, G.-C. Ahn, P.K. Hanumolu, S.-H. Lee*, S.-H. Kim*, S.-B. You*, J.-W. Kim*, G.C. Temes, U.-K. Moon, Oregon State University, Corvallis, OR, *Samsung Electronics, Yongin, Korea

19.2 – 3:50 p.m.
A 1.2V, 10.8mW, 500kHz Sigma-Delta Modulator with 84dB SNDR and 96dB SFDR, C.W. Tsang, Y. Chiu*, B. Nikolic, Univ. of California, Berkeley, CA, *University of Illinois, Urbana-Champaign, IL

19.3 – 4:15 p.m.
A 14-bit 5MS/s Continuous-Time Delta-Sigma A/D Modulator, Z. Li, T.S. Fiez, Oregon State University, Corvallis, OR

19.4 – 4:40 p.m.
An 11-bit 330MHz 8X OSR Σ-Δ Modulator for Next-Generation WLAN, J. Paramesh[1,2], R. Bishop[2], K. Soumyanath[2], D. Allstot[1], [1]University of Washington, Seattle, WA, [2]Intel Corp., Hillsboro, OR

19.5 – 5:05 p.m.
A 4GHz 4th-order Passive LC Bandpass Delta-Sigma Modulator with IF at 1.4GHz, L. Luh, J.F. Jensen, C.-M. Lin, C.-T. Tsen, D. Le, A.E. Cosand, S. Thomas, C. Fields, HRL Laboratories LLC, Malibu, CA

SESSION 20 – TAPA III
Oscillators and Dividers

Friday, June 16, 3:25 p.m.
Chairpersons: F. Dai, Auburn University
H. Yamazaki, Fujitsu Laboratories Ltd.

20.1 – 3:25 p.m.
A 20-GHz Injection-Locked LC Divider with a 25-% Locking Range, T. Shibasaki, H. Tamura*, K. Kanda*, H. Yamaguchi*, J. Ogawa*, T. Kuroda, Keio University, Yokohama, Japan, *Fujitsu Laboratories Ltd., Kawasaki, Japan

20.2 – 4:15 p.m.
Coupled Inverter Ring I/Q Oscillator for Low Power Frequency Synthesis, J. Xu, S. Verma, T.H. Lee, Stanford University, Stanford, CA

20.3 – 3:50 p.m.
Injection-Locked Frequency Dividers Based on Ring Oscillators with Optimum Injection for Wide Lock Range, A. Mirzaei, M.E. Heidari, R. Bagheri, S. Chehrazi, A.A. Abidi, University of California, Los Angeles, CA

20.4 – 4:40 p.m.
A Single-Tank Dual-Band Reconfigurable Oscillator, R. Gharpurey, T.-L. Hsieh, S. Venkatraman*, University of Texas, Austin, TX, *Texas Instruments Inc., Dallas, TX

20.5 – 5:05 p.m.
A 40-GHz Wide-Tuning-Range VCO in 0.18-μm CMOS, J.-C. Chien, L.-H. Lu, National Taiwan University, Taipei, Taiwan

SESSION 21 – TAPA I
Advanced Memory and Circuits

Saturday, June 17, 8:30 a.m.
Chairpersons: S. Natarajan, Emerging Memory Technologies, Inc.
K. Kajigaya, Elpida Memory, Inc.

21.1 – 8:30 a.m.
A 128Mb Floating Body RAM(FBRAM) on SOI with Multi-Averaging Scheme of Dummy Cell, T. Ohsawa, T. Higashi*, K. Fujita, K. Hatsuda, N. Ikumi, T. Shino, H. Nakajima, Y. Minami, N. Kusunoki, A. Sakamoto**, J. Nishimura, T. Hamamoto, S. Fujii, Toshiba Corp., *Toshiba Microelectronics Corp., **Toshiba Information Systems Corp., Yokohama, Japan

21.2 – 8:55 a.m.
A Configurable Enhanced T^{2}RAM Macro for System Level Power Management Unified Memory, K. Arimoto, F. Morishita, I. Hayashi, T. Gyohten, H. Noda, T. Ipposhi, K. Dosaka, Renesas Technology Corp., Hyogo, Japan

21.3 – 9:20 a.m.
A 3-Transistor DRAM Cell with Gated Diode for Enhanced Speed and Retention Time, W.K. Luk, J. Cai, R.H. Dennard, M.J. Immediato, S.V. Kosonocky, IBM T.J. Watson Research Center, Yorktown Heights, NY

21.4 – 9:45 a.m.
Low Power SOC Design Using Partial-Trench-Isolation ABC SOI (PTI-ABC SOI) for Sub-100-nm LSTP Technology, O. Ozawa, K. Fukuoka, Y. Igarashi, T. Kuraishi, Y. Yasu, Y. Maki, T. Ipposhi, T. Ochiai, M. Shirahata, K. Ishibashi, Renesas Technology Corp., Tokyo, Japan

21.5 – 10:10 a.m.
A Register File with 8.4GHz Throughput for Efficient Instruction Scheduling in a Pentium® 4 Processor, N. Nintunze, G. Pham, Intel Corp., Hillsboro, OR

10:35 a.m. Break

SESSION 22 – TAPA II
Equalization Techniques

Saturday, June 17, 8:30 a.m.
Chairpersons: A. Amerasekera, Texas Instruments
T. Sekiguchi, Hitachi, Ltd.

22.1 – 8:30 a.m.
A 5-mW 6-Gb/s Quarter-Rate Sampling Receiver with a 2-Tap DFE Using Soft Decisions, K.-L.J. Wong, A. Rylyakov*, C.-K.K. Yang, University of California, Los Angeles, CA, *IBM T J. Watson Research Center, Yorktown Heights, NY

22.2 – 8:55 a.m.
A Low-Power Receiver with Switched-Capacitor Summation DFE, A. Emami-Neyestanak, A. Varzaghani*, J. Bulzacchelli, A. Rylyakov, C.-K.K. Yang*, D. Friedman, IBM T.J. Watson Research Center, Yorktown Heights, NY, *University of California, Los Angeles, CA

22.3 – 9:20 a.m.
A 10-Gb/s CMOS Merged Adaptive Equalizer/CDR Circuit for Serial-Link Receivers, S. Gondi, B. Razavi, University of California, Los Angeles, CA

22.4 – 9:45 a.m.
A 200Mb/s-2Gb/s Oversampling RX with Digitally Self-Adapting Equalizer in 0.18µm CMOS Technology, G.W. den Besten, F. Gerfers*, J. Conder*, A.J. Köllmann*, P. Petkov*, Philips Research, Eindhoven, The Netherlands, *Philips Semiconductor, Eindhoven, The Netherlands

22.5 – 10:10 a.m.
A Tunable Passive Filter for Low-Power High-speed Equalizers, R. Sun, J. Park, F. O'Mahony*, C. P. Yue, Carnegie Mellon University, Pittsburgh, PA, *Intel Corp., Hillsboro, OR

10:35 a.m. Break

SESSION 23 – TAPA III
UWB

Saturday, June 17, 8:30 a.m.
Chairpersons: B. Zhao, Skyworks
M. Ugajin, NTT Microsystem Integration Labs

23.1 – 8:30 a.m.
A 2.3mW Baseband Impulse-UWB Transceiver Front-end in CMOS, I.D. O'Donnell, R.W. Brodersen, University of California, Berkeley, CA

23.2 – 8:55 a.m.
A 1-V 299μW Flashing UWB Transceiver Based on Double Thresholding Scheme, A. Tamtrakarn, H. Ishikuro*, K. Ishida, M. Takamiya, T. Sakurai, University of Tokyo, Tokyo, Japan, *Toshiba Corp., Kawasaki, Japan

23.3 – 9:20 a.m.
A Single-chip Gaussian Monocycle Pulse Transmitter using 0.18μm CMOS Technology for Intra/Interchip UWB Communication, P.K. Saha, N. Sasaki, T. Kikkawa, Hiroshima University, Hiroshima, Japan

23.4 – 9:45 a.m.
An 11-Band 3.4 to 10.3 GHz MB-OFDM UWB Receiver in 0.25μm SiGe BiCMOS, A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez, E. Sanchez-Sinencio, Texas A&M University, College Station, TX

23.5 – 10:10 a.m.
A 1.5V 9-Band CMOS Synthesizer for MB-OFDM UWB Transceivers, H. Zheng, A.W.L. Ng, H.C. Luong, The Hong Kong University of Science and Technology, Kowloon, Hong Kong

10:35 a.m. Break

SESSION 24 – TAPA I
Reducing Power, Noise, and Leakage

Saturday, June 17, 10:50 a.m.
Chairpersons: K. Roy, Purdue University
K. Kobayashi, Kyoto University

24.1 – 10:50 a.m.
Supply Voltage Adjustment Technique for Low Power Consumption and its Application to SOCs with Multiple Threshold Voltage CMOS, H. Okano, T. Shiota, Y. Kawabe, W. Shibamoto, T. Hashimoto, A. Inoue, Fujitsu Laboratories Ltd., Kawasaki, Japan

24.2 – 11:15 a.m.
The Circuits and Robust Design Methodology of the Massively Parallel Processor Based on the Matrix Architecture, H. Noda, T. Tanizaki, T. Gyohten, K. Dosaka, M. Nakajima, K. Mizumoto, K. Yoshida, T. Iwao, T. Nishijima, Y. Okuno, K. Arimoto, Renesas Technology Corp., Hyogo, Japan

24.3 – 11:40 a.m.
A Power-Managed Protocol Processor for Wireless Sensor Networks, M. Sheets, F. Burghardt, T. Karalar, J. Ammer, Y.H. Chee, J. Rabaey, University of California, Berkeley, CA

24.4 – 12:05 p.m.
A Leakage Management System Based on Clock Gating Infrastructure for a 65-nm Digital Base-Band Modem Chip, F. Jumel, P. Royannez, H. Mair, D. Scott, A.E. Rachidi, R. Lagerquist, M. Chau, S. Gururajarao, S. Thiruvengadam, M. Clinton, V. Menezes, R. Hollingsworth, J. Vaccani, F. Piacebello, N. Culp, J. Rosal, M. Ball, F. Ben-Amar, L. Bouetel, O. Domerego, J.L. Lachese, C. Fournet-Fayard, J. Ciroux, C. Raibaut, U. Ko, Texas Instruments Inc., Villeneuve Loubet, France

24.5 – 12:30 p.m.
Distributed Active Decoupling Capacitors for On-Chip Supply Noise Cancellation in Digital VLSI Circuits, J. Gu, R. Harjani, C. Kim, University of Minnesota, Minneapolis, MN

SESSION 25 – TAPA II
Nyquist ADCs II

Saturday, June 17, 10:50 a.m.
Chairpersons: K. Gulati, BitWave Semiconductor
M. Nagata, Kobe University

25.1 – 10:50 a.m.
A 15b-Linear, 20MS/s, 1.5b/Stage Pipelined ADC Digitally Calibrated with Signal-Dependent Dithering, Y.-S. Shu, B.-S. Song, University of California, San Diego, CA

25.2 – 11:15 a.m.
A 12b 10MS/s Pipelined ADC Using Reference Scaling, G. Ahn, P.K. Hanumolu, M. Kim, S. Takeuchi*, T. Sugimoto*, K. Hamashita*, K. Takasuka*, G. Temes, U. Moon, Oregon State University, Corvallis, OR, *Asahi Kasei Microsystems, Atsugi, Japan

25.3 – 11:40 a.m.
A 12b, 75MS/s Pipelined ADC Using Incomplete Settling, E. Iroaga, B. Murmann, Stanford University, Stanford, CA

25.4 – 12:05 p.m.
A 1V 30mW 10b 100MSample/s Pipeline A/D Converter Using Capacitance Coupling Techniques, K. Honda, F. Masanori, S. Kawahito, Shizuoka University, Hamammatsu, Japan

25.5 – 12:30 p.m.
A 10b 170MS/s CMOS Pipelined ADC Featuring 84dB SFDR without Calibration, J. Li, G. Manganaro, M. Courcy, B.-M. Min, L. Tomasi*, A. Alam*, R. Taylor*, National Semiconductor, Salem, NH, *National Semiconductor, Phoenix, AZ

SESSION 26 – TAPA III
RF Front Ends and Baseband Processing

Saturday, June 17, 10:50 a.m.
Chairpersons: A. Abidi, University of California, Los Angeles
M. Ito, Renesas Technology

26.1 – 10:50 a.m.
A 0.5 V 900 MHz CMOS Receiver Front End, N. Stanic, P. Kinget, Y. Tsividis, Columbia University, New York, NY

26.2 – 11:15 a.m.
Multi-band (1-6GHz), Sampled, Sliding-IF Receiver With Discrete-Time-Filtering in 90nm Digital CMOS Process, H. Lakdawala, J. Zhan, A. Ravi, S. Anderson, B.R. Carlton, R.B. Nicholls, N. Yaghini, R.E. Bishop, S.S. Taylor, K. Soumyanath, Intel Corp., Hillsboro, OR

26.3 – 11:40 a.m.
A Cartesian-Feedback Linearized CMOS RF Transmitter for EDGE Modulation, L. Tee, E. Sacchi*, R. Bocock, N. Wongkomet, P.R. Gray, University of California, Berkeley, CA, *STMicroelectronics, Pavia, Italy

26.4 – 12:05 p.m.
A 1V 14mW-per-Channel Flexible-IF CMOS Analog-Baseband IC for 802.11a/b/g Receivers, P.-I. Mak, S.-P. U*, R.P. Martins**, University of Macau, Macao, China, *Chipidea Microelectronics, Ltd., Macao, China, **Instituto Superior Tecnico, Lisbon, Portugal

26.5 – 12:30 p.m.
A 31.2mW UWB Baseband Transceiver with All-Digital I/Q-mismatch Calibration and Dynamic Sampling, J.-Y. Yu, C.-C. Chung, H.-Y. Liu, Y.-W. Lin, W.-C. Liao, T.-Y. Hsu, C.-Y. Lee, National Chiao-Tung University, Taiwan

GENERAL INFORMATION

SCOPE OF SYMPOSIUM

The Symposium covers all aspects of VLSI circuits, such as digital, analog, and mixed digital-analog circuits: such as processors, ASICs, RF, A/D and D/A converters, interface circuits, etc.; memory circuits: such as static memory, non-volatile memory, cache memory, dynamic memory, and new concepts in memories based on quantum mechanics effects, magnetism, polymers, etc.; system architecture, circuits and building blocks for networking applications; circuits, functional blocks using quantum dots, MEMS, sensors, etc.; fundamentals related to the above, including design automation tools, innovative circuits and device structures of VLSI circuits, such as: digital, analog, and mixed digital-analog.

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The VLSI Symposia encourages all participants to register on-line. To register on-line, go to www.vlsisymposium.org. All payments must be paid in US dollars by credit card or check. No bank transfers are allowed. The deadline to register is May 22, 2006. **After May 22, 2006 you must register on-site. If you register on-site, an additional $75 will be added to the registration fees.**

Payment of the registration fee entitles the registrant to one copy of the Technical Digest, one CD-ROM, all coffee breaks, one banquet and one reception ticket.

	Member	NonMember	Students
Tech Short Course	$270	$295	$75
Tech Symposium	$500	$550	$250
Tech/Circ Symposia	$950	$1,000	$350
*Circ Short Course***	*$325*	*$350*	*$100*
Circ Symposium	$500	$550	$250
Proceedings	$75	$75	$75
Add'l Short Course books	$95	$95	$95
Banquet Tickets	$75	$75	$75

*(**This year the Circuits Short Course is comprised of two programs, Analog and Digital. The cost of the short course includes both programs and attendees will receive one book for both programs. Attendees will be able to move back and forth between the two programs.)*

REGISTRATION: Credit Cards (MasterCard/Visa), personal checks, company checks or traveler's checks payable to the 2006 VLSI Symposia **in U.S. Dollars** are the only acceptable forms of payment. All checks must be drawn on U.S. banks. Registration not conforming to these guidelines will be returned. Please complete the Registration Card (see centerfold) and return with payment of the appropriate registration fees **no later than May 22, 2006** to VLSI c/o ESU, PO Box 32862, Baltimore, MD 21282, USA
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Garden View	$206.00
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All rooms are subject to an 11.41% combined tax. To make a room reservation, go to www.vlsisymposium.org, click the tab at the top of the screen labeled Travel/Reservation Information. Click on the link for the hotel reservations.

OR, complete the Hotel Reservation Form and return it directly to the Hilton Hawaiian Village no later than May 13, 2006. All reservations must be accompanied by advanced deposit or guaranteed by a credit card in order to guarantee the reservation. A confirmation will be mailed to you directly by the hotel. Check-in time is 2:00 pm and check-out is 11:00 am.

The hotel offers both non-smoking and handicapped rooms. Please make these specific requests when you make your hotel reservation.

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SYMPOSIA REGISTRATION DESK: The Symposia Registration Desk, located in the Palace Lounge Lobby will be open as follows:

Symposium on VLSI Technology

Sunday, June 11	5:00 pm - 8:00 pm
Monday, June 12	8:00 am - 5:00 pm
Tuesday, June 13	7:30 am - 5:30 pm
Wednesday, June 14	7:30 am - 5:00 pm
Thursday, June 15	7:30 am - 5:00 pm

Symposium on VLSI Circuits

Wednesday, June 14	7:30 am - 5:00 pm
Thursday, June 15	7:30 am - 5:00 pm
Friday, June 16	7:30 am - 5:00 pm
Saturday, June 17	7:30 am - 12:00 noon

VLSI CIRCUITS SYMPOSIUM RECEPTION: A reception will be held on Wednesday, June 14 from 6:00 pm to 8:00 pm on the Lagoon Green.

VLSI CIRCUITS SYMPOSIUM BANQUET: The 2006 Symposium on VLSI Circuits Banquet will be held on Friday, June 16 on the Lagoon Green from 7:00 pm to 9:00 pm. Banquet tickets for accompanying guests can be purchased at the Registration desk in the Palace Lounge Lobby.

SPEAKER PREPARATION CENTER: There will be a designated Speaker Preparation Room. Specifics will be available at the Registration Desk located in the Palace Lounge Lobby.

PROCEEDINGS: Registrants will receive (1) copy of the Proceedings and (1) copy of the CD-Rom when they pick up their Symposium materials at the Registration Desk. Additional copies of the Proceedings will be available on-site for $75. Following the Symposium, additional copies of the Proceedings will be available through IEEE Single Copy Sales, 445 Hoes Lane, Piscataway, NJ 08855, USA +1 732-981-0060 or (Toll free) 1 800-678-4333.

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