Thursday, June 15, 10:25 a.m.
Chairpersons: M.-R. Lin, AMD
H. Wakabayashi, NEC Corp.

19.1 – 10:25 a.m.

High Performance Dual Metal Gate CMOS with High Mobility and Low Threshold Voltage Applicable to Bulk CMOS Technology, S. Yamaguchi, K. Tai, T. Hirano, T. Ando, S. Hiyama, J. Wang, Y. Hagimoto, Y. Nagahama, T. Kato, K. Nagano, M. Yamanaka, S. Terauchi, S. Kanda, R. Yamamoto, Y. Tateshita, Y. Tagawa, H. Iwamoto, M. Saito, N. Nagashima, S. Kadomura, Sony Corporation, Kanagawa, Japan

We demonstrate a dual metal gate CMOS technology with HfSix for nMOS and Ru for pMOS on HfO_2 gate dielectric. These gate stacks show high mobility at Tinv=1.7nm and symmetrical low Vt equivalent to poly-Si/SiO_2. As a result, high drive currents of 780uA/um (265uA/um) at Ioff=1nA/um are achieved for Vdd=1.0V in Lg=60nm nMOS (pMOS). We also demonstrate Ion improvement of Ru/HfO_2 pMOS using (110)-substrate. As a result, excellent drive current of 400uA/um is achieved.

19.2 – 10:50 a.m.

Low Power CMOS Featuring Dual Work Function FUSI on HfSiON and 17ps Inverter Delay, T. Hoffmann, A. Veloso, A. Lauwers, H. Yu, M. Van Dal, H. Tigelaar, T. Chiarella, C. Kerner, R. Mitsuhashi, I. Satoru, M. Niwa, A. Rothschild, B. Froment, J. Ramos, A. Nackaerts, S. Brus, C. Vrancken, P.P. Absil, M. Jurczak, J.A. Kittl, S. Biesemans, IMEC, Leuven, Belgium

We report record unloaded ring oscillator delay (17ps at VDD=1.1V and 20pA/um Ioff) using low power CMOS transistors with Ni-based fully silicided (FUSI) gates on HfSiON. This result comes from two key advancements over our previous report [1]. First, we have improved the devices Idsat to be 560/245uA/um for nMOS/pMOS at an Ioff=20pA/um and VDD=1.1V. Second, we demonstrate that the use of metal gates enables a reduction of the junction anneal temperature, yielding an Lgmin reduction of 7nm/14nm for nMOS/pMOS over our Poly-Si/SiON reference. We also report for the first time that metal gate on HfSiON devices can outperform optimized conventional Poly-Si/SiON devices by up to 25% in unloaded ring oscillator.

19.3 – 11:15 a.m.

High-Performance Low Operation Power Transistor for 45nm Node Universal Applications, M. Shima, K. Okabe*, A. Yamaguchi*, T. Sakoda, K. Kawamura*, S. Pidin*, M. Okuno, T. Owada*, K. Sugimoto*, J. Ogura*, H. Kokura*, H. Morioka*, T. Watanabe*, T. Isome*, K. Okoshi*, T. Mori*, Y. Hayami*, H. Minakata, A. Hatada, Y. Shimamune, A. Katakami, H. Ota*, T. Sakuma*, T. Miyashita, K. Hosaka, H. Fukutome, N. Tamura, T. Aoyama, K. Sukegawa*, M. Nakaishi*, S. Fukuyama*, S. Nakai*, M. Kojima*, S. Sato, M. Miyajima*, K. Hashimoto*, T. Sugii, Fujitsu Laboratories Ltd., Tokyo, Japan, *Fujitsu Limited, Tokyo, Japan

High-performance low operation power (LOP) transistors were developed for 45nm node universal applications. A high uni-axial strain and low resistance NiSi technique, enhanced by a slit under the slim and high young's modulus offset spacer covered with dual stress liner, were used for electron and hole mobility enhancement and parasitic resistance reduction. As a result, the best Ion-Ioff tradeoff characteristics were obtained among the recent LOP transistors.

19.4 – 11:40 a.m.

55nm CMOS Technology for Low Standby Power/Generic Applications Deploying the Combination of Gate Work Function Control by HfSiON and Stress-Induced Mobility Enhancement, H. Nakamura*, Y. Nakahara, N. Kimizuka, T. Abe, I. Yamamoto, T. Fukase, T. Nakayama, K. Taniguchi, K. Masuzaki*, K. Uejima*, T. Iwamoto*, T. Tatsumi*, K. Imai, NEC Electronics Corporation, Kanagawa, Japan, *NEC Corporation, Kanagawa, Japan

A 55nm node Low Standby Power/Generic CMOS technology is demonstrated. The transistor deploys the combination of high-k gate dielectric film and process-induced stress technologies. It features high drive currents with low leakage, wide coverage of transistor performance and process simplicity. Ion of 525/295 µA/µm at Ioff of 20 pA/µm and Ion of 780/400 µA/µm at Ioff of 3 nA/µm with supply voltage of 1.2 V have been achieved. A leading-edge ArF immersion lithography has been utilized for fine-pitch design rules such as L/S of 160 nm for Metal 1 layer. A 0.432 μm^2 SRAM cell shows a sufficient SNM of 130 mV at supply voltage of 0.8 V.