

SESSION 8 – TAPA I  
Strain Enhanced CMOS I

Wednesday, June 14, 8:30 a.m.

Chairpersons: T. Grider, Texas Instruments  
T. Hiramoto, University of Tokyo

**8.1 – 8:30 a.m.**

**Stress Proximity Technique for Performance Improvement with Dual Stress Liner at 45nm Technology and Beyond**, X. Chen, S. Fang, W. Gao<sup>1</sup>, T. Dyer, Y. W. Teh<sup>1</sup>, S. S. Tan<sup>1</sup>, Y. Ko<sup>3</sup>, C. Baiocco, A. Ajmera, J. Park<sup>3</sup>, J. Kim<sup>3</sup>, R. Stierstorfer<sup>2</sup>, D. Chidambarao, Z. Luo, N. Nivo, P. Nguyen, J. Yuan, S. Panda, O. Kwon<sup>2</sup>, N. Edleman, T. Tjoa<sup>1</sup>, J. Widodo<sup>1</sup>, M. Belyansky, M. Sherony, R. Amos, H. Ng, M. Hierlemann<sup>2</sup>, D. Coolbough, A. Steegen, I. Yang, J. Sudijono<sup>1</sup>, T. Schiml<sup>2</sup>, J. H. Ku<sup>3</sup>, C. Davis, IBM Semiconductor Research and Development Center, Hopewell Junction, NY, <sup>1</sup>Chartered Semiconductor Manufacturing, <sup>2</sup>Infineon Technologies AG, <sup>3</sup>Samsung Electronics Co. Ltd.

Integration of stress proximity technique (SPT) and dual stress liners (DSL) has been demonstrated for the first time. It maximizes the strain transfer from nitride liner to the channel. PFET drive current improvements of 20% for isolated and 28% for nested poly gate pitch devices have been achieved with SPT. Leading edge PFET Ion=660uA/um at Ioff=100nA/um at 1V Vdd operation is demonstrated without using embedded SiGe junctions. Inverter ring oscillator delay is reduced by 15% with SPT.

**8.2 – 8:55 a.m.**

**1-D and 2-D Geometry Effects in Uniaxially-Strained Dual Etch Stop Layer Stressor Integrations**, P. Grudowski, V. Adams, X.-Z. Bo, K. Loiko, S. Filipiak, J. Hackenberg, M. Jahanbani, M. Azrak, S. Goktepli, M. Shroff, W.-J. Liang\*, S.J. Lian\*, V. Kolagunta, N. Cave, C.-H. Wu\*, M. Foisy, H.C. Tuan\*, J. Cheek, Freescale Semiconductor Inc., Austin, TX, \*Taiwan Semiconductor Manufacturing Company

We report, for the first time, on the 2-D boundary effects in a high performance 65nm SOI technology with dual Etch Stop Layer (dESL) stressors. 1-D geometry effects, such as poly pitch dependence, and the implications on SPICE models and circuit design are also discussed. It will be shown that PMOS and ring oscillator performance can be significantly enhanced by optimizing the transverse and lateral placement of the dESL boundary.

**8.3 – 9:20 a.m.**

**Scalable eSiGe S/D Technology with Less Layout Dependence for 45-nm Generation**, K. Ota, T. Sanuki\*, K. Yahashi\*, Y. Miyanami, K. Matsuo\*, J. Idebuchi\*, M. Moriya, K. Nakayama\*, R. Yamaguchi\*, H. Tanaka\*, T. Yamazaki, S. Terauchi, A. Horiuchi, S. Fujita, I. Mizushima\*, H. Yamasaki\*, K. Nagaoka, A. Oishi\*, Y. Takegawa\*, K. Ohno, M. Iwai\*, M. Saito, F. Matsuoka\*, N. Nagashima, Sony Corporation, Kanagawa, Japan, \*Toshiba Corporation, Kanagawa, Japan

We developed a less layout-dependent epitaxially grown SiGe(eSiGe) S/D technique for PFET by analyzing the layout dependence of the mobility-enhancement mechanism. In addition, we succeeded in increasing the drive current by improving the eSiGe structure and the impurity profile. We also obtained a high drive current of 750 uA/um at Vdd=1V, Ioff=100nA/um.

**8.4 – 9:45 a.m.**

**50 nm Silicon-On-Insulator N-MOSFET Featuring Multiple Stressors: Silicon-Carbon Source/Drain Regions and Tensile Stress Silicon Nitride Liner**, K.-W. Ang, K.-J. Chui, H.-C. Chin, Y.-L. Foo<sup>^</sup>, A. Du\*, W. Deng\*, M.-F. Li, G. Samudra, N. Balasubramanian\*, Y.-C. Yeo, National University of Singapore, Singapore, \*Institute of Microelectronics, Singapore, <sup>^</sup>Institute of Materials Research & Engineering, Singapore

A novel n-channel strained SOI transistor featuring silicon-carbon (SiC) source/drain (S/D) regions and tensile stress silicon nitride (SiN) liner is demonstrated for the first time. Drive current Idsat enhancement contributed by the dual stressors is found to be additive and a significant increase in Idsat of 55% is observed at a gate length of 50 nm. In addition, we report the dependence of drive current on channel orientation, with highest Idsat observed for strained n-MOSFETs with the [010] channel direction. A study of the carrier transport characteristics indicate reduced channel back-scattering and enhanced carrier injection velocity due to the strain effects.